Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation

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***Abstract*—This paper proposes, for the first time, the concept of programmable logic circuit realized with single-electron transistors (SETs). An SET having nonvolatile memory function is a key element for the programmable SET logic. The writing and erasing operations of the nonvolatile memory function make it possible to tune the phase of Coulomb oscillations. The half-period phase shift induced by the memory function makes the function of SETs complementary to that of the conventional SETs. As a result, SETs having nonvolatile memory function have the functionality of both the conventional (nMOS-like) SETs and the complementary (pMOS-like) SETs. By utilizing this fact, the function of SET circuits can be programmed with great flexibility, on the basis of the information stored by the memory functions. We have successfully fabricated SETs that operate at room temperature and observed the highest room-temperature peak-to-valley current ratio of Coulomb oscillations. The operation of the programmable SET logic is demonstrated using the room-temperature operating SETs. This is the first demonstration of room-temperature SET logic operation. The proposed programmable SET logic provides the potential for low-power, intelligent LSI chips suitable for mobile applications.**

***Index Terms*—Coulomb blockade, memories, programmable logic devices, quantum dots (QDs), quantum effect semiconductor devices, silicon on insulator technology, single-electron phenomena.**

I. Introduction

In the scaling of CMOS transistors into the deep sub-50-nm regime, both fundamental limits and technological challenges are encountered. In order to extend the prodigious progress of LSI performance in this regime, it is essential to introduce into future LSIs new devices having an operation principle, which is more effective at smaller dimensions than is the operation principle currently employed. Single-electron transistors (SETs) [1] are promising candidate for new nanoscaled devices, because SETs has the good scalability as well as the low-power property.

However, in order to introduce SETs in practical LSIs, it is necessary to realize SETs that can operate at room temperature. In addition, it is essential to develop the design methodology of SET logic circuit, by which the functionality of SET logic circuit can surpass that of the conventional CMOS logic circuits.

As for the room-temperature operation, many attempts have been made to realize room-temperature operating SETs [2]–[6]. However, the peak-to-valley current ratio (PVCR) of Coulomb oscillations is still smaller than one decade. This small PVCR makes it difficult to demonstrate SET circuit operation at room temperature. As a result, although several successful examples of SET circuit operation at low temperatures have been reported [7]–[10], no room-temperature SET circuit operation has been reported so far.

As for the circuit design methodology, one common design method for SET logic circuits is to replace MOSFETs of conventional CMOS logic circuits with SETs [11]. In fact, it has been demonstrated that the selection of proper bias conditions makes it possible to construct large-scale SET logic circuits by replacing MOSFETs with SETs [9], [12]. However, the functionality of such SET logic circuits is the same as that of the CMOS logic circuits. Recently, several attempts to design SET logic circuits that have higher functionality than that of CMOS logic circuits have been reported [7], [11]. The number of such reports is very limited.

In this paper, we report, for the first time, the concept of the programmable logic circuit realized with SETs. In the proposed programmable SET logic, single-electron devices, which work not only as SETs but also as nonvolatile memories, are utilized. It is proposed that the adjustment of Coulomb oscillation phase with the nonvolatile memory function offers high programmability for LSI. This high programmability cannot be achieved by MOSFETs even if the MOSFETs have nonvolatile memory function. At room temperature, the operation of the programmable SET logic is demonstrated using room-temperature operating SETs having room-temperature nonvolatile memory function.

II. Programmable SET Logic

A. Principle

The principle of the programmable SET logic is firstly introduced. In the programmable SET logic, a SET with a nonvolatile memory function (NVM) works as a key element. Since charges around the quantum dot (QD) of the SET, namely an SET island, shift the phase of Coulomb oscillations, the writing/erasing operations of the memory function, which inject/eject charges to/form the memory node near the SET

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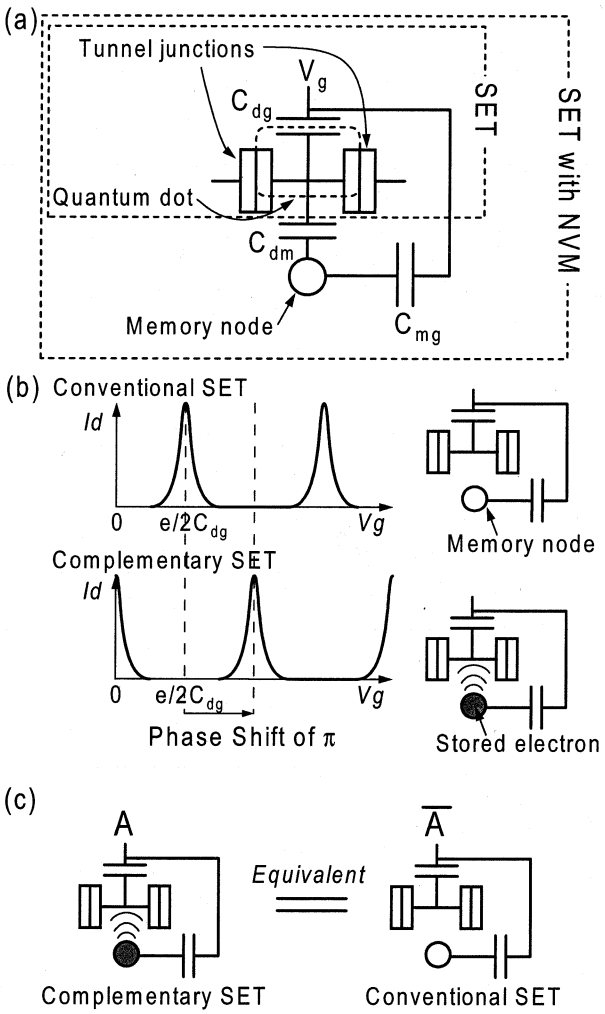

Fig. 1. Principle of programmable SET logic. (a) Schematic of an SET with nonvolatile memory function (NVM) that is a key element of the programmable SET logic. The SET with NMV consists of a QD, tunnel junctions, and a memory node. Here, C_{dg}, C_{mg}, C_{dm}, I_d, and V_g are the capacitance between the QD and the gate electrode, the capacitance between the memory node and the gate electrode, the capacitance between the QD and the memory node, the drain current, and the gate voltage, respectively. (b) Characteristics of SET with NVM. Initially, the SET with NVM shows the same Id-Vg characteristics as those of the conventional SET (upper figure). The complementary SET (lower figure) is realized after writing operation generating the half-period (π) phase shift of Coulomb oscillations. For simplicity, C_{dm} is not shown in the schematics of SETs with NVM. (c) Logical meaning of complementary SET. The operation of the complementary SET is equivalent to that of conventional SET to which logically inverted signal is fed.

island, make it possible to tune the phase of Coulomb oscillations. If the amount of the injected charges is adequate, the phase shift becomes the half period of the Coulomb oscillations. Fig. 1(a) shows the schematic of the SET with NVM. Fig. 1(b) shows the way to change the function of SETs by using the phase shift due to the memory function. As shown in Fig. 1(b), the phase shift of half period (π) makes the function of SETs complementary to that of the conventional SETs. As a result, SETs having NVM have the functionalities of both conventional (nMOS-like) SETs and complementary (pMOS-like) SETs. It should be noted that the nMOS-like SETs having logical input of A are functionally the same as the pMOS-like SETs having logical input of NOT A [Fig. 1(c)]. By utilizing this fact, the function of SET circuits can be programmed with great flexibility, based on the information stored by the memory functions.

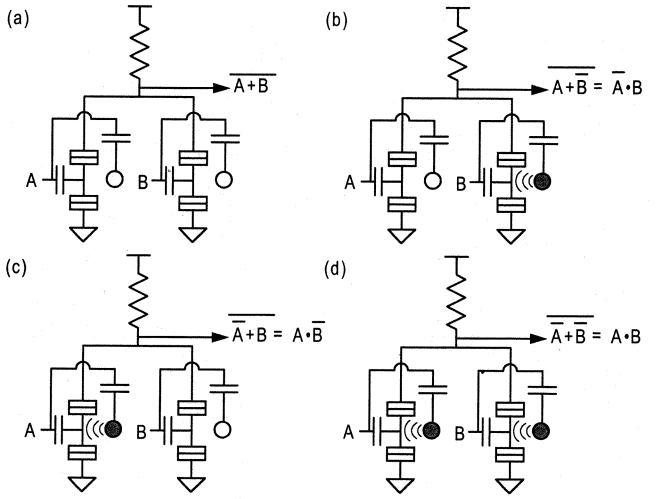

Fig. 2. Example of programmable SET logic. The circuit consists of a resistor load and parallel SETs with nonvolatile memory function. (a) Both the SETs perform as conventional SETs, and the circuit works as a NOR gate. (b), (c) One of the SETs performs as a complementary SET. (d) Both the SETs perform as complementary SETs, and the circuit works as an AND gate.

As described above, in the programmable SET logic, the concept similar to the complementary SETs proposed by Tucker [11] is utilized. The difference between Tucker's complementary SET concept and the programmable SET logic concept is that in the programmable SET logic the phase shift is realized not by a fixed gate voltage applied to the second gate but by a nonvolatile memory function. Therefore, we can arbitrarily select the function of SETs from both complementary one and conventional one by using the memory function, which contrasts with the case of Tucker's complementary SETs, where the function of each SET is fixed.

In the programmable SET logic, the adjustment of Coulomb oscillation phase by the memory function is utilized. Although the similar concept has been proposed previously [14], the function of the SET is adjusted and fixed to a desired function there. As a result, each SET works only as an nMOS-like SET or only as a pMOS-like SET. On the contrary, in the present programmable SET logic, the function of SETs can be changed from a pMOS-like/nMOS-like SET to a nMOS-like/pMOS-like SET arbitrarily and dynamically.

Fig. 2 shows an example of programmable SET logic circuits. The circuit consists of two parallel pull-down SETs having nonvolatile memory function. The function of the logic can be selected from the four logic operations shown in Fig. 2, including the NOR operation and the AND operation, by programming the function of SETs with the memory functions. It should be noted that this high programmability could never be realized by MOSFETs, even though they have nonvolatile memory function. Fig. 3 shows the simulated waveforms of the programmable SET logic operating as the AND logic gate as well as the NOR logic gate. The simulation is performed with the circuit

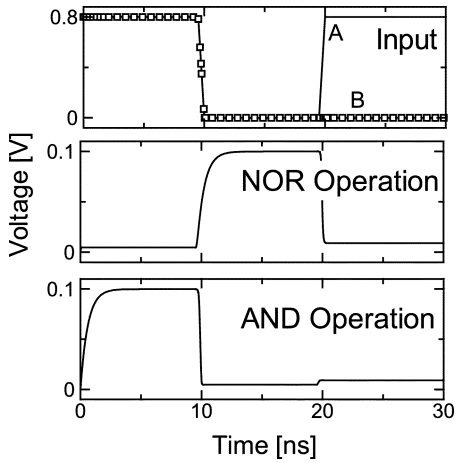

Fig. 3. Simulated waveform of the programmable SET logic shown in Fig. 2. The total capacitance C_{Σ}, the gate capacitance $C_{\rm g}$, and the source and drain capacitance C_T are assumed to be 0.32, 0.1, and 0.06 aF, respectively. The tunneling resistance of 500 kΩ, the load resistance of 20 MΩ, and the output load capacitance of 30 aF are also assumed.

simulator SPICE, where the analytical SET model [15] is implemented. The successful operation of the programmable SET logic is confirmed.

B. Array Structure

In order to realize arbitrary combinational logic function, we propose here the SET programmable logic array (SET-PLA) concept. The programmable logic array (PLA) concept is one of the common, important concepts to implementing arbitrary logic functions in a regular, structured way. In the conventional PLA [16], [24] double-rail inputs (each independent variable and its complement) are fed to the AND plane that calculate the needed product terms consisting of the input variables or their complements ANDed together, and these product terms are then fed to the OR plane, where they are ORed together. In FET technologies, both the AND plane and the OR plane are usually realized with two NOR planes, because a NOR gate with all inputs inverted logically realizes the AND function and NOR-NOT cascade realizes the OR function. One way to program the PLA is whether an FET connecting an interconnect is placed (activated) or not.

Fig. 4 shows the two-input SET-PLA. The important point for the SET-PLA is that, when the SETs having NVM are used as switching devices, single-rail input is sufficient to construct the arbitrary logic functions, because of the dual functionality of the SETs having NVM. In the SET-PLA, FET-type SETs, which turn completely off at the gate voltages lower than the FETs threshold voltage, V_{th}, are utilized (Fig. 5). These FET-type SETs are made in semiconductor materials such as silicon and have n^{+} source/drain regions and a p^{-} channel region including a QD as well as tunnel junctions. Therefore, the FET-type SETs are the combination of MOSFETs and SETs, meaning that they turn off at the gate voltage lower than the V_{th} of MOSFETs and turn on at the gate voltage higher than the V_{th} of MOSFETs and that the turn-on-current oscillates as gate voltage increases. The FET-type SETs have already been realized by many authors [2]–[4], and moreover our SETs discussed later are also the FET-type SETs. The writing operation inducing the phase shift

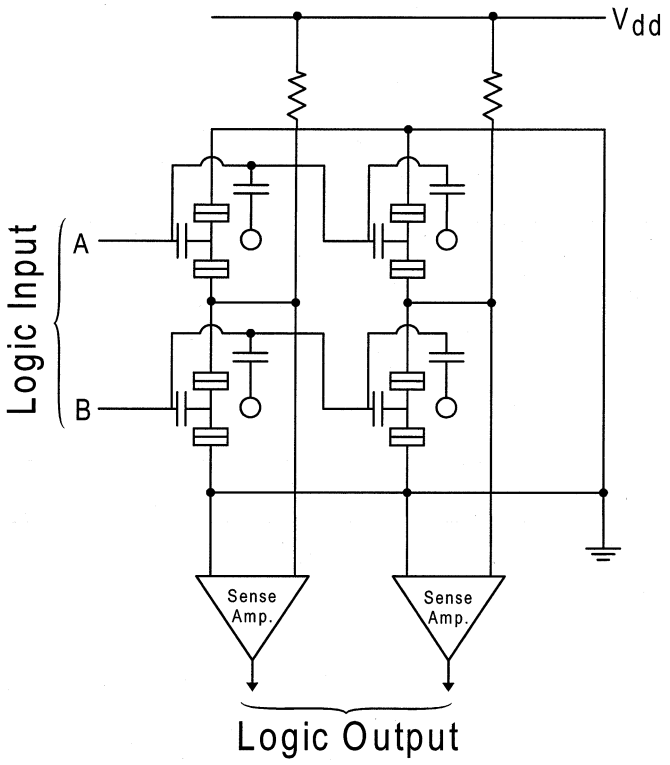

Fig. 4. Schematic of SET-PLA. Vdd is the supply voltage for SETs. Vdd should be smaller than the logical "high" level in order to suppress the strong DIBL-like effects observed in SETs [12]. The sense amplifiers amplify the output voltage of SETs to match the logic levels.

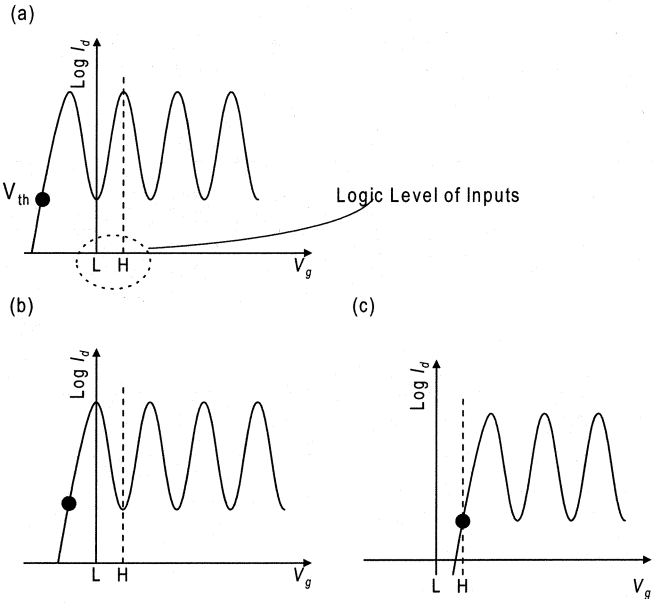

Fig. 5. Characteristics of FET-type SET with nonvolatile memory function, which is used in SET-PLA before writing operation (a), after writing operation inducing the phase-shift of half period (b), and after writing operation inducing the phase-shift of one period (c). The closed circle indicates the threshold voltage V_{th} of the FET.

of half period (π) makes the function of SETs complementary to that of the conventional SETs, and logically realizes the complementary input. The writing operation inducing the phase shift of one period (2π) logically realizes the disconnection of the line

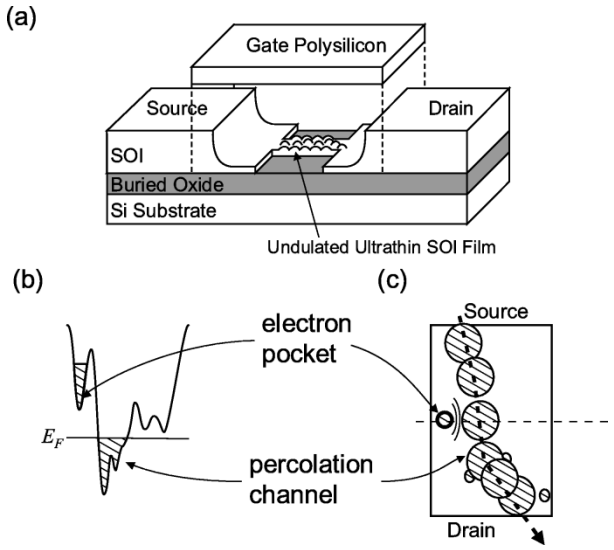

Fig. 6. (a) Structure of fabricated SET with nonvolatile memory function (NVM). (b) Potential profile in undulated SOI film.

(interconnect), because in this case the SET with NVM turns off at the gate voltages of both "high" level and "low" level. As a result, the PLA can be realized without dual-rail inputs but with single-rail inputs in the SET-PLA, and thus the number of devices and interconnects can be reduced to the half.

In view of the disadvantages of SETs as the switching devices in LSIs, the SET-PLA has the following advantages.

i) Since the SET-PLA consists of NOR SET arrays, all the SETs are connected in *parallel* and not in series. This is a great advantage from the viewpoint of the speed because SETs inherently have high output resistance.
ii) Since the SET-PLA has an array structure, sense amplifiers, which amplify the small output of SETs [12], can be implemented easily (Fig. 4).
iii) The dynamic logic style, which is suitable for SETs to construct large logic systems [12], can be used in the SET-PLA.

III. Fabrication of Room-Temperature Operating SET

As the structure of the SET with NVM, a MOSFET in an undulated ultrathin silicon-on-insulator (SOI) film is utilized [17]. The structure is illustrated in Fig. 6(a). As shown in the figure, the device structure is almost the same as that of conventional SOI MOSFETs, but the SOI film has two key features: 1) its surface is intentionally undulated in nanoscaled dimensions as shown in Fig. 6(a) by utilizing an alkaline-based solution; 2) the channel SOI thickness is thinned to a few nanometers [17]. The nanoscaled undulation in the ultrathin film results in the formation of nanoscaled potential fluctuations due to the difference of quantum confinement effects from one part to another. Consequently, both the narrow electron channel through potential valleys and small potential pockets, storing memory information, are formed in the film as shown in Fig. 6(b). Since potential fluctuations still exist in the narrow channel, the channel effectively splits into several QDss. Thus, the percolation channel works

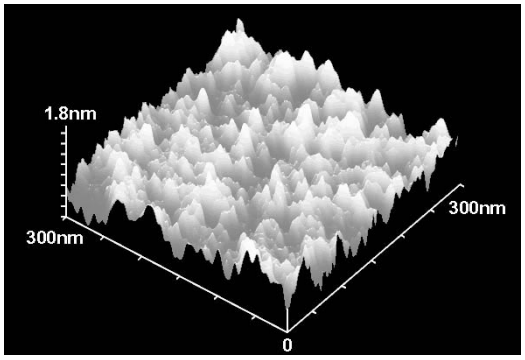

Fig. 7. Atomic-force microscope (AFM) image of undulated SOI film.

as a single-electron transistor having nearby the electron pocket working as a memory node [17].

We previously reported the successful fabrication of this type of SET with NVM [17]. Although Coulomb oscillations were observed only at temperatures lower than room temperature, nonvolatile memory functions were observed even at room temperature. The measurements of the undulation with atomic force microscopy revealed that the undulation had two correlation lengths. Based on the analysis of electrical characteristics, it was concluded that the Coulomb blockade oscillations were dominated by a QD formed by the longer-correlation-length undulation, and single-electron memory effects were due to QDs formed by the shorter-correlation-length undulation [17].

Therefore, in order to raise the temperature at which Coulomb oscillations are observable, shortening of the longer correlation is effective. In this report, we utilize hydrogen peroxide as the etching inhibitor in place of surfactants [17] and eliminate the HF treatment just before the alkaline-based solution dip. Fig. 7 shows an atomic-force-microscope (AFM) image of the undulated silicon surface. From the height-difference correlation function analysis [17], [18], it is shown that the short-range correlation length is 4 nm, and furthermore it is revealed that we have succeeded in shortening the long-range correlation length of the undulation from 15.4 to 11.7 nm, which is sufficiently small to observe the room-temperature Coulomb oscillations. However, it should be noted that in the present AFM image long-range correlation length is not observed clearly, meaning that, in the present undulation, the long-range correlation length is the upper limit of the undulation period rather than the correlation length of the gentle undulation containing the small, rapid undulations [17]. As a result, in the present device, the size of the QD dominating the single-electron transport is in the range between the short-range correlation length and the long-range correlation length.

Fig. 8 shows the drain current I_d versus gate voltage V_g characteristics of a fabricated device at various temperatures. The oscillating I_d characteristics against V_g, namely Coulomb oscillations, are clearly observed. As shown in the figure, the peak-to-valley current ratio (PVCR) of 2.62 is obtained. In order to estimate the size of the QD dominating the single-electron transport, we derive the analytical PVCR of the Coulomb oscillations as a function of the temperature normalized by the single-electron charging energy in the dot. First, the minimum zero-bias

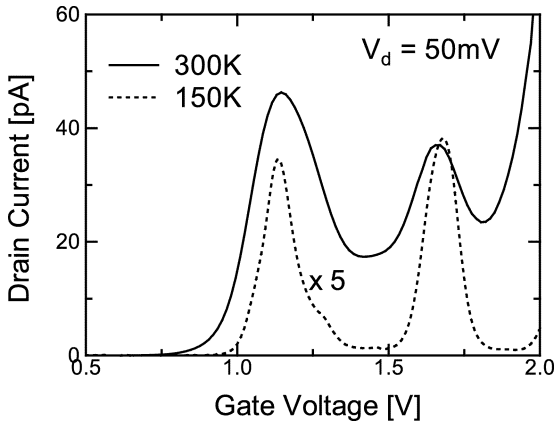

Fig. 8. I_d versus V_g characteristics of a fabricated SET at various temperatures. Coulomb oscillation characteristics are clearly observed even at room temperature.

conductance $G_{\min}$ of the Coulomb oscillations can be derived by solving 3×3 matrix master equation

$$G_{\min} = \lim_{V \to 0} \frac{I_{\min}}{V} = \frac{1}{R_T} \frac{1}{\widetilde{T}\left[1 - \cosh\left(\frac{1}{\widetilde{T}}\right) + 3\sinh\left(\frac{1}{\widetilde{T}}\right)\right]} \tag{1}$$

where $I_{\min}$ is the valley current, R_T is the resistance of the tunnel junctions, $\widetilde{T}$ is the normalized temperature. The normalized temperature $\widetilde{T}$ is defined as

$$\widetilde{T} = \frac{2C_\Sigma k_B T}{e^2} \tag{2}$$

where C_Σ is the total capacitance of the dot, k_B is the Boltzman constant, T is the temperature, and e is the elementary charge. Since the maximum zero-bias conductance, G_{max}, of the Coulomb oscillations can be well approximated as $4R_T$, when $\widetilde{T}$ is less than 0.3. The PVCR is analytically expressed as

$$\mathrm{PVCR} = \frac{G_{\max}}{G_{\min}} = \frac{1}{4}\widetilde{T}\left[1 - \cosh\left(\frac{1}{\widetilde{T}}\right) + 3\sinh\left(\frac{1}{\widetilde{T}}\right)\right]. \tag{3}$$

From (2), (3), and PVCR of 2.62 at 300 K, the total capacitance C_Σ of the QD is estimated to be 0.86 aF. Assuming that the dot has a circular disk-shape and is completely surrounded by SiO_2, the diameter of the dot is estimated to be 6.3 nm from the self-capacitance calculation. The estimated diameter is within the range between the short-range correlation length and the long-range correlation length. Thus, it is concluded that the QD dominating single-electron transport is generated by the nanoscaled undulation in the ultrathin SOI film.

Fig. 9 shows the characteristics of another device at room temperature. In Fig. 9(a), Coulomb staircase characteristics are clear observed. Although, in narrow semiconductor wires, other conductance oscillation mechanisms such as variable-range hopping [19] are discussed, staircase characteristics shown in Fig. 9(a) suggest that conductance oscillations in our devices are due to Coulomb blockade effects. In Fig. 9(b), Coulomb oscillations with PVCR of 10^2 are clearly observed. This is the highest PVCR among the room-temperature operating SETs reported so far. From the PVCR, the total capacitance is estimated to be 0.38 aF. The diameter of the SET island is estimated to be 2.8 nm, when the energy level quantization is neglected.

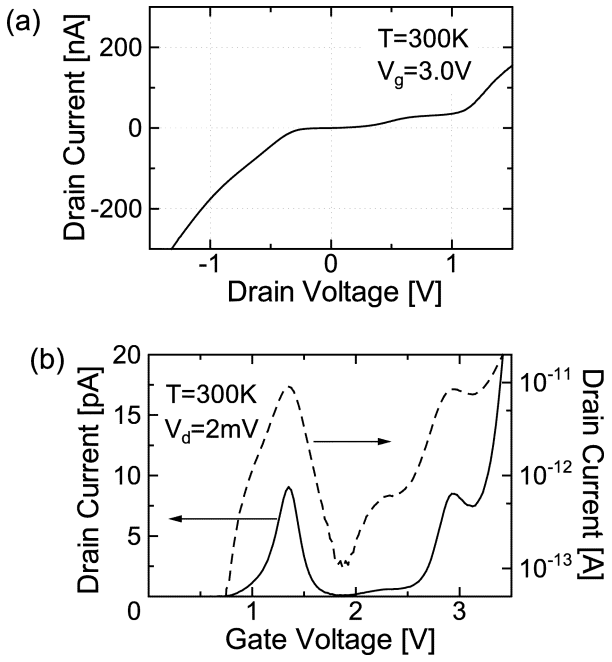

Fig. 9. Room temperature characteristics of another SET. (a) $I_d - V_d$ and (b) $I_d - V_g$ characteristics are shown. It should be noted that a Coulomb staircase as well as Coulomb oscillations with peak-to-valley current ratio (PVCR) of 10^2 are clearly observed.

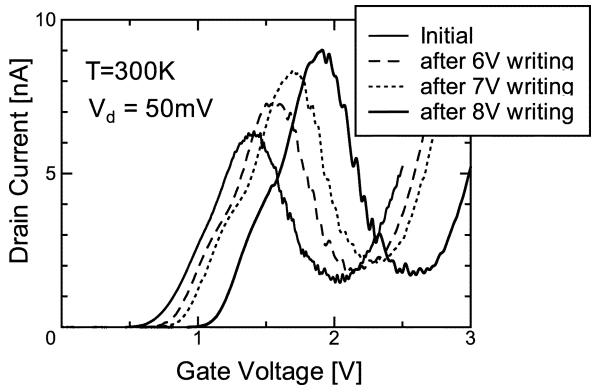

Fig. 10. Phase shift of the Coulomb oscillations induced by applying writing voltages.

However, if the energy level quantization is taken into account, the diameter is estimated to be approximately 4 nm, which is equivalent to the short-range correlation length of the undulation. In addition, the quantization energy and the charging energy are calculated to be 0.07 eV and 0.14 eV, respectively. Therefore, it is considered that in this device the SET island is formed by the short-range-correlation-length undulation.

The memory function is observed in the form of the shift of the $I_d - V_g$ characteristics by applying the writing voltage, as shown in Fig. 10. Fig. 11 shows the typical retention characteristics of the memory function. The retention time of greater than 10^2 seconds are clearly observed. It is considered that the step-like discharging corresponds to a single-electron discharging.

IV. Demonstration of Programmable SET Logic

In this section, we show the demonstration of room-temperature operation of the proposed programmable SET logic. The operation is demonstrated using a test circuit consisting of a SET

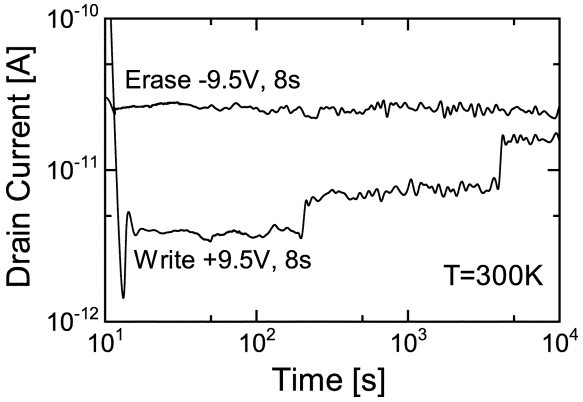

Fig. 11. Retention characteristics of memory function by applying 9.5 V writing pulse with eight-second width and −9.5 V erasing pulse with 8-s width. The current was measured at the gate voltage of 0 V after applying the writing/erasing pulse. Steplike discharging characteristics are observed.

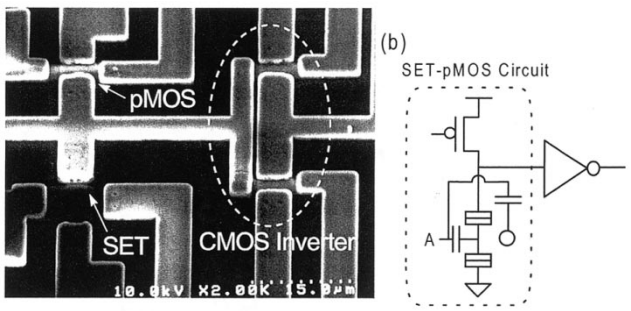

Fig. 12. (a) Scanning electron microscope (SEM) photograph of the fabricated circuit consisting of an SET with NVM, a pMOSFET load, and a CMOS inverter. (b) Circuit schematic of (a).

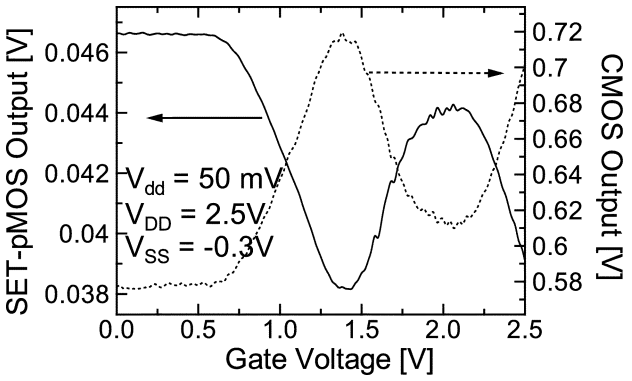

Fig. 13. Output voltage of the SET-pMOS circuit and the CMOS inverter as a function of the gate voltage of the SET. The SET conductance oscillations are perfectly reproduced. The small output signal of the SET-pMOS circuit is successfully amplified with the CMOS inverter.

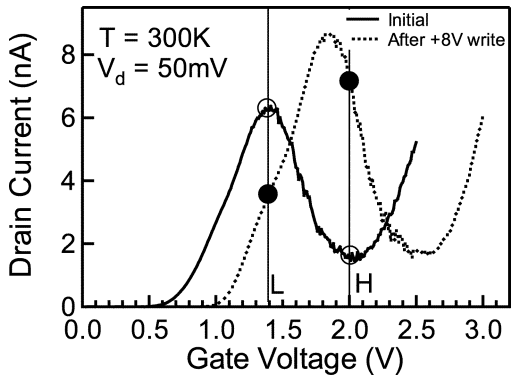

Fig. 14. Bias conditions for the demonstration of programmable SET logic operation of the SET-pMOS circuit. The low and high levels of the SET inputs are selected to be 1.4 and 2.0 V, respectively.

with NVM as an active device, a pMOSFET load, and a CMOS inverter on a chip, as shown in Fig. 12. The characteristics of the SET in the circuit are shown in Fig. 10. Fig. 13 shows the output voltages of the SET-pMOS circuit and the CMOS inverter as a function of the gate voltage of the SET. As shown in the figure, the Coulomb oscillations of the SET are successfully reproduced as the output of the SET-pMOS circuit, and the output is amplified with the CMOS inverter. In order to compensate for the low driving-capability disadvantage of SETs, the integration of CMOS with SETs is indispensable for the practical use of SETs in LSIs [12], [20]–[23]. This is not only the first demonstration of SET circuit operation but also the first on-chip-level demonstration of SET/CMOS hybrid circuit operation.

Here, we demonstrate the programmable operation of the SET-pMOS circuit. The function of the SET-pMOS circuit is programmed from a converter/inverter to an inverter/converter using the nonvolatile memory function. As shown in Fig. 10, the phase control of Coulomb oscillation is possible by using the nonvolatile memory function. Since the retention time of the memory is greater than 10^2 seconds, the memory function can be utilized to transform the function of the SET as well as that of the SET-pMOS circuit.

We firstly show the circuit operation before applying writing voltage to the SET gate. As shown in Fig. 14, the low and high levels of SET inputs are selected to be 1.4 and 2.0 V, respectively. When the gate voltage is 1.4 V/2.0 V (low/high), the current level of the Coulomb oscillation becomes high/low, and the output of the SET-pMOS circuit becomes low/high level. Therefore, the waveform of the SET-pMOS circuit is synchronized with that of the SET input as shown in Fig. (15a) and (b) (the solid line), meaning that the SET-pMOS circuit acts as a converter.

After applying writing voltage, the current levels of Coulomb oscillations become low and high at the SET inputs of 1.4 and 2.0 V, respectively (Fig. 14). Consequently, the waveform of the SET-pMOS circuit is inverted to that of the SET input as shown in Fig. 15(a) and (b) (the dashed line), meaning that the SET-pMOS circuit acts as an inverter. Thus, we have experimentally demonstrated the multifunctional operation, namely a converter operation and an inverter operation, of the SET-pMOS circuit at room temperature.

V. Conclusion

In this paper, we propose the concept of the programmable SET logic circuit, which has higher programmability than that of the programmable logic circuit realized with the conventional CMOS technologies. We have successfully fabricated SETs that operate at room temperature with the highest PVCR ever reported, and demonstrated the room-temperature operation of an SET circuit. It is confirmed that the function of an SET-pMOS circuit can be programmed from a converter/inverter to an inverter/converter by utilizing a nonvolatile memory function incorporated in the SET, showing that the programmable single-electron transistor logic is realized in logic circuits consisting of SETs with a nonvolatile memory function. In addition, we have

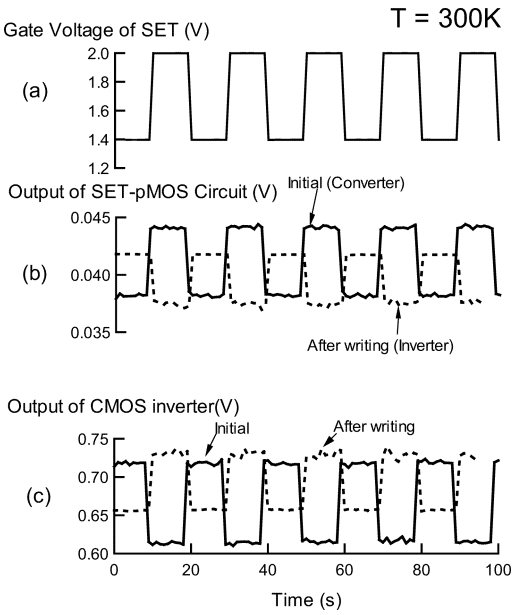

Fig. 15. Experimental room-temperature demonstration of programmable SET logic operation of the SET-pMOS circuit. (a) Waveform of the SET gate voltage. (b) Output waveform of the SET-pMOS circuit. The initial characteristics are indicated by the solid line. The characteristics after applying 8 V writing pulse are indicated by the dashed line. The initial waveform is synchronized with that of the SET gate voltage. On the other hand, the waveform after writing operation is logically inverted to that of the SET gate voltage, demonstrating that the function of the SET-pMOS circuit can be programmed from a converter to an inverter by utilizing the nonvolatile memory function. (c) Output waveform of the CMOS inverter. The waveform is logically inverted to that of the SET-pMOS circuit. It should be noted that the small output voltage of the SET-pMOS circuit is amplified with the CMOS inverter.

demonstrated, for the first time, the on-chip-level demonstration of an SET/CMOS hybrid circuit, confirming the compatibility of the fabrication process of the present SETs with that of conventional CMOS technologies. Since SETs are inherently low driving capability devices, the combination of SETs with CMOS on a chip is indispensable for the practical use of SETs. SET circuits have potential to improve LSI performance in terms of power consumption and functionality such as programmability. Therefore, the proposed programmable SET logic provides the potential for low-power, intelligent LSI chips, suitable for ubiquitous applications.

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