# Schottky-barrier heights of single-crystal $NiSi_2$ on Si(111): The effect of a surface $p$-$n$ junction

R. T. Tung, K. K. Ng, J. M. Gibson, and A. F. J. Levi
*AT&T Bell Laboratories, Murray Hill, New Jersey 07974*
(Received 20 November 1985)

Current-voltage, capacitance-voltage, and activation-energy measurements obtained for epitaxial nickel silicides grown on Si(111) have exposed the importance of the temperature used to flash-evaporate oxide off the surface prior to metal deposition. Near-ideal behavior is found for Schottky barriers grown on substrates cleaned at $\sim$820 °C in ultrahigh vacuum. The Fermi-level positions at the interfaces of single-crystal type-$A$ and type-$B$ $NiSi_2$ are shown to differ by greater than 100 meV. Transmission electron microscopy demonstrated the epitaxial perfection of these silicide layers. At a cleaning temperature of 1050 °C, the apparent Schottky-barrier heights increased substantially for substrates with a doping concentration of $N_D$ less than approximately $10^{15}$ cm$^{-3}$. This increase is due to the conversion of the $n$-type semiconductor surface region to $p$ type during the 1050 °C anneal. The presence of this $p$-$n$ junction results in a high apparent Schottky-barrier height ($\gtrsim$0.75 eV) which no longer bears an immediate relationship to the interface Fermi-level position. Recent discrepancies reported by different groups concerning the barrier heights of $NiSi_2$ on Si(111) are attributed to this effect.

## I. INTRODUCTION

During recent years, there has been growing interest in delineating the systematics of Schottky-barrier (SB) formation.[1–3] Despite this effort, it is not yet possible to either predict or explain the magnitudes of the Schottky-barrier height (SBH) associated with different metal-semiconductor interfaces. A major obstacle has been the lack of direct experimental information correlating the SBH with relevant interface physical parameters. In an ordinary transport measurement at a polycrystalline metal-semiconductor junction, electrons travelling through different parts of the interface may experience different local barriers because of the inhomogeneity in the interface structure and associated electronic properties. An average SBH is measured which contains little information regarding the relationship between local electronic and structural properties. Such information, critical to understanding the microscopic SB mechanism, is washed out in the averaging process. Epitaxial single-crystal metal-semiconductor systems are a much better choice in this respect because of their homogeneity in both interface structure and electronic properties. Direct links between the observed SBH and the physical parameters can then be revealed and used to develop a SB theory.

The system consisting of $NiSi_2$ on Si(111) has been shown to be nearly perfect in epitaxial structure.[4] The atomic structure of the interface has been modeled by high-resolution transmission electron microscopy (TEM) (Refs. 5 and 6) and ion channeling (Ref. 7), making the system an ideal case for SB studies. Moreover, a unique comparison is offered in that $NiSi_2$ layers can be formed on Si(111) with either one of the two epitaxial orientations, type $A$ or type $B$.[4] $NiSi_2$ has the cubic $CaF_2$ crystalline structure and the lattice constant of $NiSi_2$ is smaller than that of silicon by $\sim$0.4% at room temperature. An $A$-type $NiSi_2$ layer has the same orientation as the Si(111) substrate, while a $B$-type layer shares the normal $\langle 111 \rangle$ axis with the substrate but is rotated 180° about this axis with respect to the substrate. With the observed interface structure differing only by third-nearest-neighbor atoms and beyond, the $A$ and $B$ interfaces are identical in all bulk parameters which are thought to affect the SBH. The experimentally determined interface atomic positions are accurate to $\sim$0.1 Å; however, a substantial difference of 140 meV between SBH's of type $A$ and type $B$ was observed experimentally.[8] This was a significant discovery because the variation of SBH with orientation was not in agreement with previous SBH experiments on polycrystalline systems and was also in conflict with the predictions of many existing SB models. A mechanism of intrinsic nature is suggested by such a correlation of SBH with details of the interface microstructure.

Recently, Liehr, Schmidt, LeGoues, and Ho[9] challenged the results of the original SBH measurements and claimed that there is no difference in the SBH's of the type-$A$ and type-$B$ layers. Since it is very important to clarify this issue, the present study was undertaken in order to identify potential sources for the disparity. Particular emphasis has been placed on identifying variables associated with sample processing which differed in the previously reported works and understanding the manner in which such variables might influence the analysis of data used to extract a value for the Schottky-barrier height. It was found that a doping-compensation phenomenon occurring under the experimental conditions of Liehr *et al.*[9] was capable of dominating the electrical environment near the interface and bringing the apparent SBH's of type $A$ and type $B$ close together. When such spurious effects are absent, the SBH's of type-$A$ and type-$B$ $NiSi_2$ are shown to differ by 120–140 meV as claimed in our original work.[8]

 ©1986 The American Physical Society

TABLE I. Sample-preparation parameters for thin $NiSi_2$ on Si(111).

| | Substrate resistivity (Ω cm) | Dopant | Diode delineation | Substrate cleaning *ex situ* | Substrate cleaning *in situ* | Silicide reaction temperature (°C) | Silicide thickness (Å) | Orientation determination | Schottky-barrier height measurement[b] |
|---|---|---|---|---|---|---|---|---|---|
| Tung (Ref. 11) | 0.2–1.3 | As,P | Oxide windows | methanol | <1000 °C 2 min | ~500 | 60–800 | LEED channeling | *I-V* *C-V* |
| Liehr *et al.* (Ref. 9) | 8–12 | P | Metal mask | ethanol | 1100 °C seconds | 450–500 | 60–120 | Cross-section TEM | *I-V* PR |
| This work | 0.2–25 | As,P | Oxide windows and etched plateaus | Shiraki cleaning | ~820 °C and ~1050 °C 2 min[a] | 400–500 | 60–900 | LEED channeling TEM | *I-V* *C-V* AE |

[a] 10-sec heating at 1050 °C was also used.
[b] PR, photoresponse; AE, activation-energy method.

## II. EXPERIMENTAL PROCEDURES

### A. Sample preparation

A comparison of published preparation parameters relevant to the two works is presented in Table I. This study has emphasized an examination of two parameters which differed substantially in the reports by Tung[8] and Liehr *et al.*[9] The first of these is the substrate doping concentration, which has been varied between $N_D = 1\times10^{14}$ and $3\times10^{16}$ $cm^{-3}$ in this study in order to overlap the substrate-resistivity range employed previously. Boron-doped *p*-type substrates were also used. The second parameter is the thermal processing temperature $T_{cl}$ used to clean the Si substrate of contaminants prior to metal deposition. Liehr *et al.*[9] employed a brief (~10 sec), high-temperature flash around 1100 °C, whereas Tung used temperatures below 1000 °C. In the present work substrate cleaning at two temperatures, $T_{cl} \sim 820$ and 1050 °C, has been examined using substrates cleaned *ex situ* by the Shiraki method.[10] The duration of the flash was varied from 10 sec to 2 min. The temperature was measured by optical pyrometry and was estimated to be accurate to ±25 °C. Substrates not cleaned by the Shiraki technique were also used to provide a comparison. A few substrates were given a brief HF etch and rinsed with methanol to deliberately increase the surface carbon content.

The detailed procedures utilized in sample preparation under ultrahigh-vacuum (UHV) conditions (base pressure $\sim 1\times10^{-10}$ Torr) are similar to those employed in previous works.[11,12] Arrays of circular windows with diameters of 127–635 μm are photolithographically defined in the (3000–5000)-Å-thick $SiO_2$ layer grown on Si. Large regions not covered by oxide, ~3 mm wide, are available on every sample. These areas, which are also metallized during the silicide growth, facilitate *in situ* characterization by Auger-electron spectroscopy (AES) and low-energy electron diffraction (LEED), and eventually provide space for Rutherford backscattering spectroscopy (RBS) and TEM analyses. A few experiments were performed on substrates without the oxide layer to single out potential contamination problems due to the presence of the oxide. These silicide layers were then etched into arrays of plateaus for electrical measurement.

The thickness of the $NiSi_2$ films studied was usually 60–70 Å for both *A* and *B* orientations. The *A*-oriented disilicide was formed by deposition of ~18 Å of Ni at a substrate temperature of below 100 °C followed by annealing at 450–500 °C for ~1 min.[4] The *B* orientation was obtained by depositions of ~18 Å Ni and ~50 Å Si followed by annealing at 450–500 °C, or by repeated Ni depositions (~4 Å at a time) and annealing after each deposition. Some type-*B* layers were grown by deposition of ~8–11 Å Ni and annealing. Thick (>500 Å) silicide layers were grown by deposition of Ni at ~600–650 °C on the thin template layers.[13] The major difference between thick and thin layers is the much lower density of misfit dislocations at the interfaces of the thin, pseudomorphic layers. Orientation of the silicide was preliminarily determined *in situ* with LEED.[4] After the samples had been characterized electrically, the orientation was checked by

RBS.[13] Selected samples were thinned down for TEM analysis at 200 kV accelerating voltage. In related experiments, we have studied polycrystalline NiSi and CoSi layers. They were grown by deposition of ~100–200 Å Ni or Co, respectively, and annealing to ~400 °C for 10 min. It was found that the unreacted metal on top of the $SiO_2$ was electrically isolated from the silicide and therefore no attempt was made to remove it.

*A*- and *B*-oriented $NiSi_2$ layers were grown side by side simultaneously on the same wafer, thus ensuring comparable contamination levels in the two regions. The physical layout of adjacent *A*- and *B*-oriented regions also minimizes any differences in reaction temperature during the annealing phase of silicide formation. Variations in either the annealing temperature or contamination levels have been identified previously as potential sources of low barriers.[9]

Ohmic contact was made to the entire backside of the *n*-type sample by Sb deposition (~150 Å thick), followed by laser alloying (~1.5 J/cm$^2$, 30 nsec, ruby) and Au evaporation (~1000 Å thick). On some lightly doped samples which were heated to 1050 °C, a few scribe marks were made on the backside of the sample before Ohmic contact was made. This was done as a precaution against possible *p*-*n* junction formation as we will describe. However, even without these steps, the back Ohmic contact was found to be good. On *p*-type samples, In deposition (~150 Å thick) was used (instead of Sb) to make back Ohmic contact.

### B. SBH measurements

Current-voltage (*I*-*V*) data were recorded with an *x*-*y* plotter. The linear portion of the logarithmic *I*-*V* curves was extrapolated to obtain the zero-bias saturation current $I_s$ and the diode-ideality factor $n$.[14,15] The *I*-*V* barrier height, $\phi_B^n$ or $\phi_B^p$, was obtained by assuming the single-carrier thermionic-emission expression for current transport given by

$$\phi_B^n = \frac{kT}{q} \ln \left[ \frac{AA^{**}T^2}{I_s} \right] , \quad (1)$$

where $A$ is the diode area and $A^{**}$ is the effective Richardson's constant. A value of $A^{**}$ equal to 112 and 32 $\mathrm{A\,cm^{-2}\,K^{-2}}$ was used for *n*- and *p*-type substrates, respectively. Image-force lowering was then added to $\phi_B^n$ to give the intrinsic SBH, $\phi_{B0}^n$. Richardson's plot of the saturation current in the temperature range ~150–300 K was used to determine the SBH by the activation energy method. Capacitances were measured with a *C*-*V* plotter and with a capacitance bridge. Frequencies of 40 kHz to 1 MHz were used with ~10 mV modulation voltage. Occasionally, the temperature was lowered to reduce the inphase component and allow a more accurate measurement. The *C*-*V* plotter was not used for substrate doping $N_D < 1\times10^{15}$ cm$^{-3}$ because of the potential errors involved with such instruments when capacitances are low. Under these circumstances a capacitance bridge was always used.

## III. RESULTS

The Shiraki cleaning procedure[10] was very effective in reducing the carbon content on the Si surface. After substrates were degassed at ~600 °C in UHV, the carbon 272-eV AES intensity was barely detectable, at less than 0.1% of that of the silicon *LVV* intensity. We could not positively identify any change of the carbon line intensity when oxide was flashed off the surface at ~820 °C or at ~1050 °C. No oxygen was detected after either heat treatment and sharp 7×7 patterns were observed by LEED. When degreased substrates were introduced in the chamber without the Shiraki cleaning procedures, a much higher carbon level was observed on the surface. After degassing, the carbon line was about 20% of the silicon AES line. However, following the 1050 °C annealing, the carbon AES signal also dropped to near the detection limit. Neither LEED nor AES could detect any difference in the structure and chemical content of the substrate surface prepared by these methods.

Orientations of $NiSi_2$ layers were deduced by LEED, RBS and channeling, and TEM measurements. It was found that the desired method for intentional type-*A* growth consistently gave pure type-*A* single crystals.[4] For type-*B* formation, the method of sequential Ni and Si deposition worked almost every time, while the repeated template growth method had a much lower success rate, yielding mixed *A*+*B* layers about half of the time. Because of this, the bulk of the data was obtained from type-*B* layers grown by the former method.

The most reliable method for determining the orientation and the morphology of the silicide layers is a combination of TEM plan-view and cross-section imaging. Cross-section TEM is ideally suited to study the details of the atomic structure at the interface, but is unreliable in giving information about the overall film morphology because of the very small area sampled. Of the ten samples that were examined by TEM in this study and the many more that were examined since the *A*,*B* epitaxial growth was first discovered in our laboratory, the TEM findings have always been in agreement with the LEED results. We have not seen cases where substantial mixing of grains was found in $NiSi_2$ layers when LEED had indicated a layer to be of pure orientation. When deposition conditions were deliberately changed so that a low density of *A* grains were introduced into the majority *B*-type film, LEED was able to unequivocally detect the presence of the *A* grains which occupied only about 5% of the total area (see Fig. 1). This demonstrates that LEED is a very convenient technique for silicide-orientation determination with a detection limit of better than a few percent. RBS and channeling, on the other hand, comprise a less reliable technique when trace amounts of mixed grains are concerned. Although we were reasonably confident about the silicide-orientation assignment by LEED, the absolute confirmation came from TEM analyses performed on layers where electrical measurements had been carried out.

Plan-view dark-field TEM images of typical *A* and *B* thin layers and a mixed *A*+*B* layer are shown in Fig. 2. Dark-field two-beam (113) Bragg reflections were used to

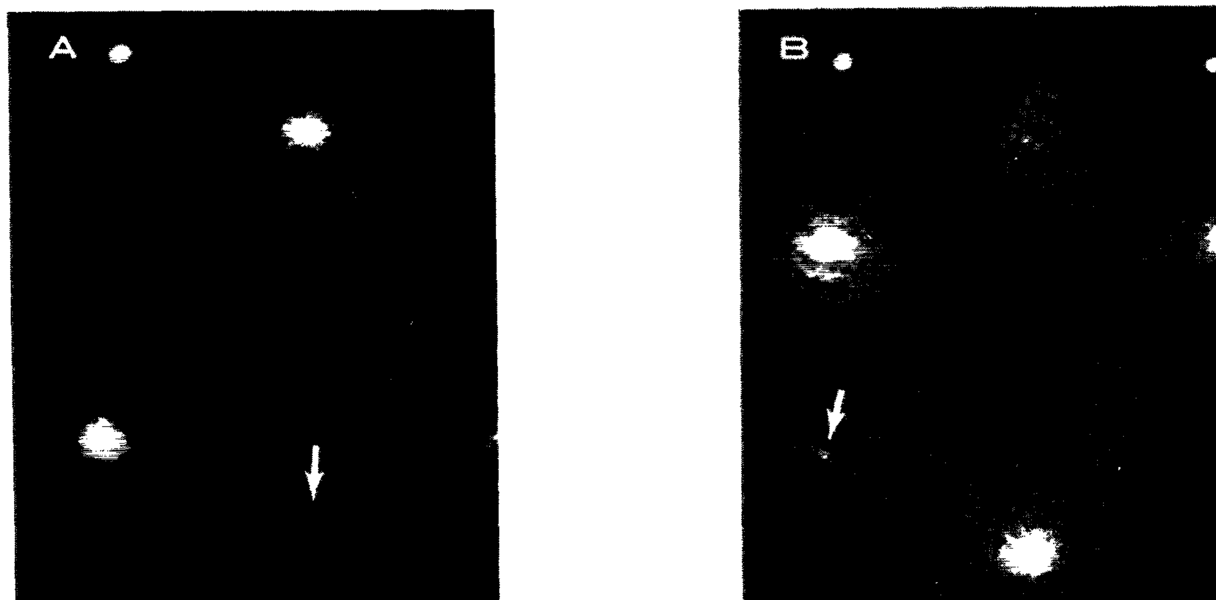


FIG. 1. Low-energy electron-diffraction pattern of the surface of a pure type-$A$ oriented $NiSi_2$ layer and an essentially type-$B$ layer with $\sim 5\%$ of the area covered by type-$A$ material. The intensity of the arrowed spots gives an indication of the percentage of area occupied by silicide of the opposite orientation.

form these images so that either $B$-type material in the $A$-type film, or vice versa, would be imaged as a bright area. The pictures demonstrate the absence of misoriented material for the type-$A$ and type-$B$ films. For the mixed $A+B$ film a $B$ reflection shows that type-$B$ grain size is $\sim 1000$ Å and that type-$B$ grains comprise less than 50% of the total area in this particular film. Figure 3 shows TEM images taken with substrate reflections which reveal both type-$A$ and type-$B$ areas and are useful in identifying defect structures and topography in the templates. All layers show occasional fine features ($\sim 1000$ Å in size) which are thought to be related to thickness nonuniformity. Only type-$B$ templates show infrequent interface dislocations, although these are absent in the thinnest films ($<35$ Å). The most important conclusion from TEM is that we can fabricate truly single-crystal layers of pure orientation; there are no detectable $B$ grains inside the $A$ films and vice versa. Secondly, the $A$-type and $B$-type layers are of similar morphology. So the difference in SBH between $A$ and $B$ interfaces cannot be explained by gross differences in interface roughness as Liehr *et al.*[9] had suggested.

The apparent SBH's of silicides were found to depend on substrate-cleaning temperature $T_{cl}$ and on the substrate-doping concentration $N_D$. Possible explanations of this phenomenon will be discussed later in this paper. Initially, SBH measurements will be presented in their respective $N_D$ and $T_{cl}$ category. For convenience, $T_{cl}$'s of

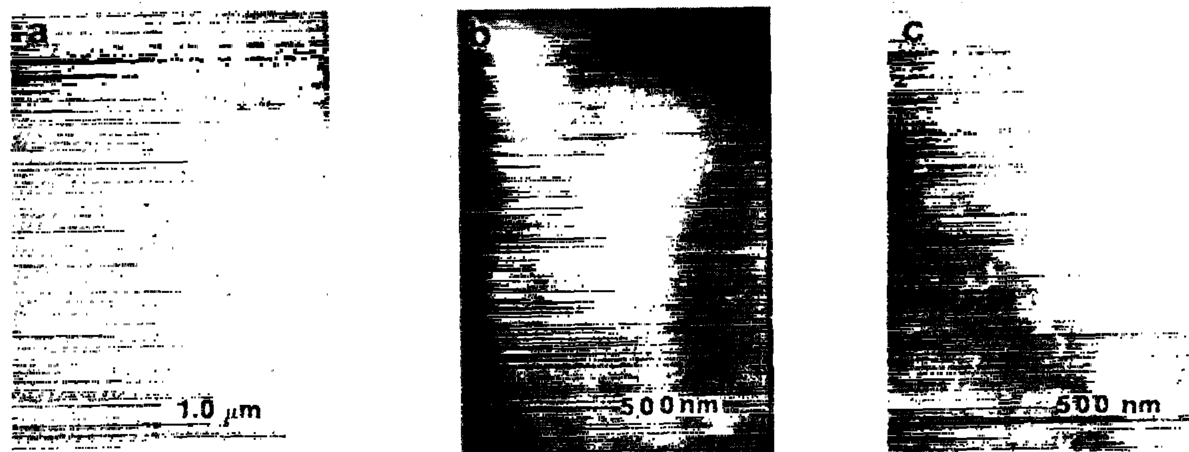


FIG. 2. Plan-view dark-field TEM images of thin (a) type-$A$, (b) type-$B$, and (c) mixed $A+B$ $NiSi_2$ template layers. Images were taken with (113) reflections, which reveal misoriented material. These demonstrate the epitaxial integrity of the type-$A$ and type-$B$ films and that the grain size of the mixed $A+B$ film is $\sim 1000$ Å. Mottled contrast in the upper part of (a) is due to damage in the thinning process.

FIG. 3. TEM images taken with substrate reflections which show both type-$A$- and type-$B$-oriented material from the same $NiSi_2$ templates in Fig. 2, respectively.

$\sim$820 and $\sim$1050 °C will be referred to as the low temperature (LT) and the high temperature (HT), respectively. Substrate-doping concentrations of $N_D \lesssim 1\times10^{15}$ cm$^{-3}$ and $N_D \gtrsim 6\times10^{15}$ cm$^{-3}$ will be referred to as lightly doped (LD) and heavily doped (HD), respectively. Three distinct categories of SBH variation can be found, namely (1) LT, (2) HT-LD, and (3) HT-HD.

### A. Substrate-cleaning temperature $\sim$820 °C (LT)

Electrical measurements of LT silicide samples essentially reproduced the results originally published on this system.[8] The $I$-$V$ behavior of type-$A$ $NiSi_2$ was very consistent and resembled an ideal Schottky diode ($n < 1.03$). A small number of diodes, either type $A$ or type $B$, had identifiable levels of recombination-generation current[15] and were excluded from the analyses. The SBH of type-$A$ diodes always fell within a narrow range of $\phi_{B0}^n = 0.66 \pm 0.01$ eV. The ideality factors of the type-$B$ $NiSi_2$ layers appeared to vary from sample to sample, ranging from 1.02 to 1.12. But the SBH's deduced from the $I$-$V$ curve still remained fairly consistent at $\phi_{B0}^n = 0.79 \pm 0.01$ eV. $C$-$V$ plots of thin $NiSi_2$ layers are shown in Fig. 4. A $\phi_{B0}^n$ of $0.65 \pm 0.01$ eV was determined for type-$A$ $NiSi_2$ from such measurements. For type-$B$ $NiSi_2$, $C$-$V$ yielded $\phi_{B0}^n = 0.79 \pm 0.02$ eV. Capacitances were found to be insensitive to the testing frequency in the range 40 kHZ to 1 MHz. This is therefore a suitable range for meaningful SBH measurements. The doping concentration deduced from the slope of the $1/C^2$ plot always agreed with the specified substrate bulk resistivity.

The SBH's of thin $NiSi_2$ layers of mixed orientation depended on the exact proportions of type-$A$ and type-$B$ areas in the films. On samples where roughly equal areas of $A$ and $B$ orientation were present, the SBH determined by $I$-$V$ measurements was similar to the pure type-$A$ films, i.e., $\phi_{B0}^n \sim 0.67$ eV. The $\phi_{B0}^n$ deduced from $C$-$V$ measurement, however, was $\sim$0.71 eV. A majority $B$-type $NiSi_2$ layer which had been determined by LEED to contain about $\sim$10% of type-$A$ grains displayed an $I$-$V$ SBH of 0.71 eV and a $C$-$V$ SBH of $\sim$0.77 eV. Occasionally, nominal $B$-type layers also displayed this behavior; it is believed that such layers contain small regions, such as type-$A$ oriented grains, of low SBH. The behavior of the mixed $A+B$ layers can be understood in terms of the coexistence of $A$-type grains with their low SBH and $B$-type grains with their high SBH. The low SBH tends to dominate the current transport in $I$-$V$ measurements, while the depletion-region width is more evenly affected by high and low SBH patches, and hence $C$-$V$ measurements tend to give an arithmetic average. Recently, direct evidence on the modulation of SBH in mixed $A+B$ $NiSi_2$ films was obtained[16] through electron-beam-induced current (EBIC) measurements in a scanning electron microscope (SEM).

$I$-$V$ behaviors of selected samples were studied below

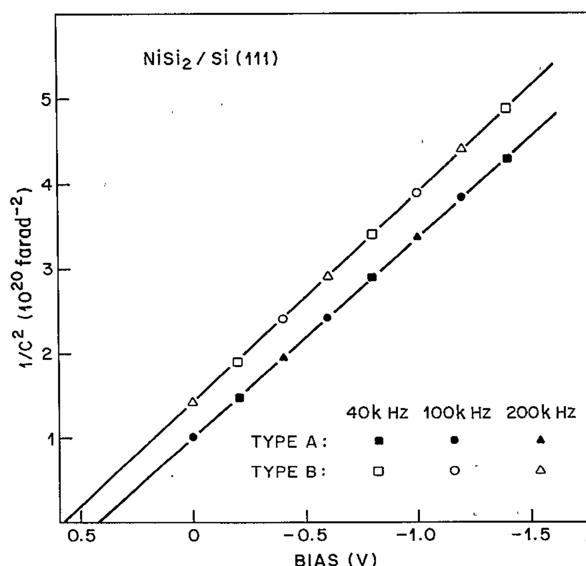


FIG. 4. $C$-$V$ plots of type-$A$ and type-$B$ $NiSi_2$, measured at three different frequencies.

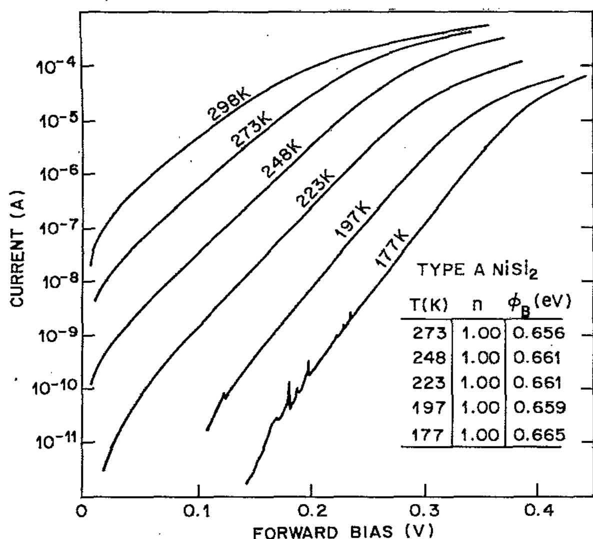


FIG. 5. Low-temperature *I-V* behavior of a type-*A* $NiSi_2$ on *n*-type Si(111). Noise at low temperature is due to the contact to silicide layer.

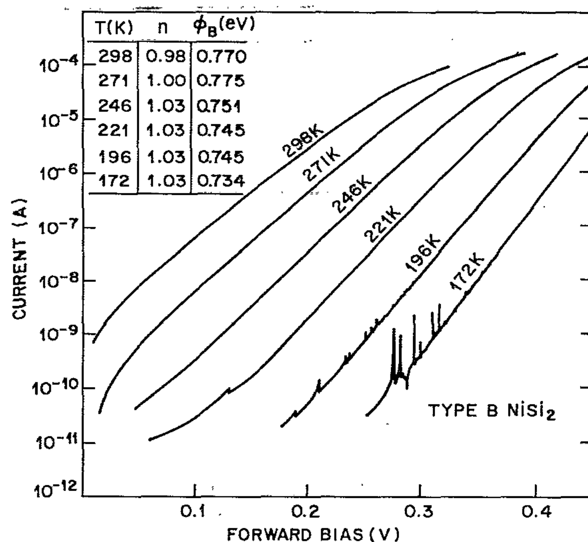


FIG. 7. Low-temperature *I-V* behavior of a type-*B* $NiSi_2$ on *n*-type Si(111).

room temperature. Typical results for a thin type-*A* $NiSi_2$ layer are shown in Fig. 5. It was found that the SBH remained constant for a wide temperature range. The slope of the *I-V* plot changed with temperature to maintain a consistently low ideality factor. The plot of $\ln(I_s/T^2)$ versus $1/T$ as shown in Fig. 6 yielded a $\phi_{B0}^n$ of 0.67 eV, which was very close to the SBH deduced from other measurements. On the average, a $\phi_{B0}^n=0.66$ eV was deduced for type-*A* $NiSi_2$ from activation-energy measurements. This agreement justified our choice of the effective Richardson's constant. The low-temperature *I-V* measurements of type-*B* $NiSi_2$ displayed more complicated behavior. Results of one example are shown in Fig. 7. There was a steady decrease of the measured $\Phi_B^n$ and a slow increase of the ideality factor as the temperature was lowered. A likely explanation of such behavior is the possible existence of very small areas of low SBH in the layer, such as the edges of the diode, type-*A* grains, dislocations, steps, etc. As the temperature was lowered, the contribution of such local weak spots to the total junction current became significant because of the $e^{-\phi_B/kT}$ factor, and a lower SBH was measured. A Richardson's plot (Fig. 6) of the saturation current yielded a $\phi_{B0}^n$ of $\sim$0.72 eV for this particular diode, and 0.73 eV on the average. Because of the difficulties just mentioned, this value should be viewed only as a lower limit of the SBH. Capacitance measurements below room temperature yielded a $\phi_{B0}^n$ of 0.79 and 0.65 eV for type-*B* and type-*A* layers, respectively, agreeing with the room-temperature results.

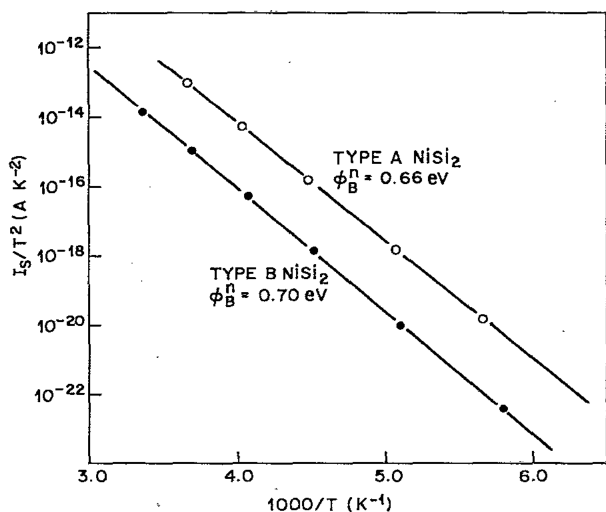


FIG. 6. Richardson's plot of the saturation current as a function of temperature. Data points were deduced from curves shown in Figs. 4 and 6, respectively, for the type-*A* and type-*B* $NiSi_2$.

The electrical behavior of plateau diodes processed from $NiSi_2$ layers grown on Si(111) without oxide patterning was essentially identical to those observed on diodes within oxide windows. Examples of *I-V* characteristics of a type-*A* $NiSi_2$ plateau diode at various temperatures are shown in Fig. 8. An activation-energy plot deduced a $\phi_{B0}^n$ of 0.65 eV for this diode. TEM analysis was then carried out in these same diodes and verified that the orientation was indeed type *A* and that no type *B* grains were present.

Previously, we have attempted SBH measurements of the $NiSi_2$ epitaxial layers on *p*-type Si(111). Nearly Ohmic behavior was found for type-*B* $NiSi_2$ and a value of $\phi_{B0}^p=0.47$ eV was obtained for type-*A* $NiSi_2$ from room-temperature *I-V* studies.[11] Because the linear regions in the log*I* plots were short, artificial corrections for the series resistance had to be made to deduce the SBH as well as the ideality factor.[11] In the present study, the uncertainty associated with curve fitting was removed by performing *I-V* measurements of these diodes at below room temperature. The reduced magnitudes of the current lessened the effect of series resistance and hence allowed more accurate measurement of the SBH. Examples are

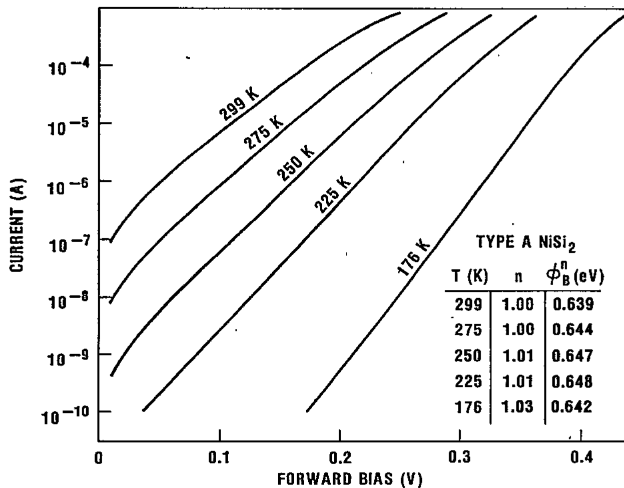


FIG. 8. Low-temperature *I-V* behavior of a plateau diode etched from a type-*A* $NiSi_2$ layer grown on *n*-type Si(111). Plateau area is $8.9\times10^{-4}$ $cm^2$.

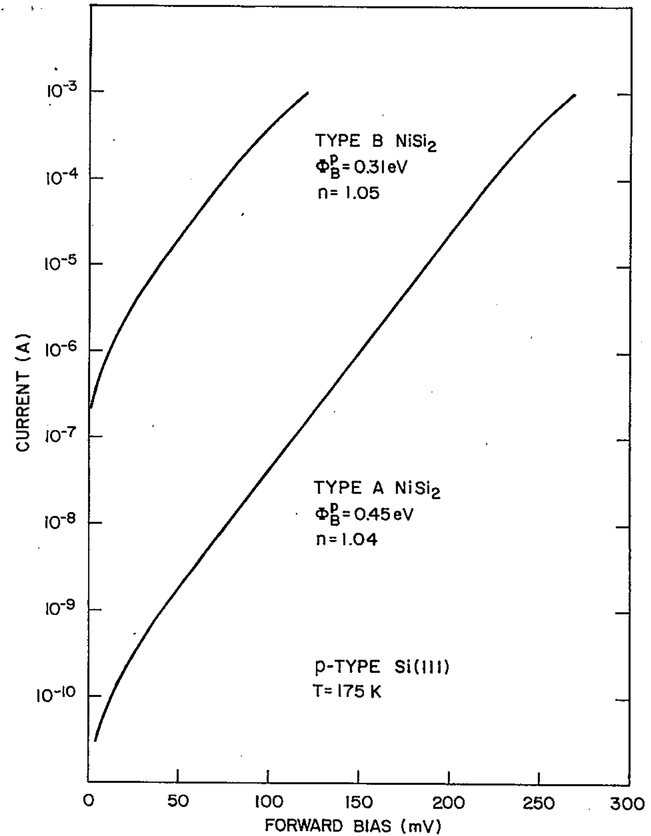


FIG. 9. *I-V* characteristics of type-*A* and type-*B* $NiSi_2$ on *p*-type Si(111). Measurements were done at below room temperature.

shown in Fig. 9. These and other data suggested a $\phi_{B0}^{p}$ of $0.47\pm0.02$ and $0.34\pm0.03$ eV for type-*A* and type-*B* $NiSi_2$, respectively. The fact that the difference between SBH's of type-*A* and type-*B* $NiSi_2$ on *p*-type substrates is about the same as the difference on *n*-type Si has very important implications. If the low SBH for type-*A* $NiSi_2$ on *n*-type Si(111) had been due to interface roughness as had been suggested,[9] regions between facets or steps should still have a high SBH. On a *p*-type substrate, these regions became "weak spots" of low SBH and should dominate the *I-V* characteristics. Therefore, the present observation of 0.47 eV for the SBH of the type-*A* $NiSi_2$ on *p*-type Si(111) argues strongly against the explanation offered by Liehr *et al.*[9] Mixed $A+B$ layers had a $\phi_{B0}^{p}$ of $\sim$0.34 eV on *p*-type Si(111), similar to the lower (type *B* in this case) of the two SBH's on this substrate. This behavior, expected from the "patch effect," showed clearly the inhomogeneity of the Fermi-level (FL) position of the mixed $A+B$ interface, in contrast to the assignment of a uniform SBH for such mixed layers by Liehr *et al.*[9]

The sum of SBH's on *p* and *n*-type substrates is very close to the band gap of Si for either *A* or *B* orientation. This suggests that the FL position for Si near the interface is independent of the doping type and differs by about $\sim$140 meV depending on whether type *A* or type *B* is in contact with it. Table II summarizes results of all the electrical measurements for samples grown on LT substrates.

As can be seen in Table II, thick layers of $NiSi_2$ have essentially the same SBH as the thin layers of the corresponding orientation. This shows that misfit dislocations do not play a major role in the determination of the interface FL position. In the growth of the thick layers, only Ni was deposited and the $NiSi_2$/Si interface moved in the direction of bulk Si. The final interface position lies $\sim$700 Å beneath the original Si surface. If we assume

TABLE II. Schottky-barrier heights of $NiSi_2$ on Si(111) cleaned at $\sim$820 °C. (AE denotes activation-energy method.)

| Orientation | Thickness (Å) | Type | $\phi_{B0}$ (eV) *I-V* | *C-V* | AE | $n^a$ |
|---|---|---|---|---|---|---|
| *A* | 60–70 | *n* | 0.66 | 0.65 | 0.66 | 1.00–1.03 |
| *B* | 60–70 | *n* | 0.79 | 0.79 | 0.73 | 1.01–1.10 |
| $A+B$ | <100 | *n* | 0.66–0.70 | 0.68–0.79 | 0.67 | 1.03 |
| *A* | 700–900 | *n* | 0.65 | 0.65 | | 1.04 |
| *B* | 700–900 | *n* | 0.79 | 0.79 | | 1.02–1.15 |
| *A* | 60–70 | *p* | 0.47 | | 0.47 | 1.01 |
| *B* | 60–70 | *p* | 0.34 | | 0.32 | 1.05 |
| $A+B$ | <100 | *p* | 0.34 | | | 1.05 |

[a]For $T\geq250$ K.

that a much lower density of deep-level impurities exists in the bulk than near the original Si surface, then the fact that thin and thick silicides have the same SBH suggests that the FL position is not determined by impurity states. Recent deep-level transient spectroscopy (DLTS) measurements have shown no evidence for defect states at epitaxial $NiSi_2$ interfaces.[17]

### B. Substrate-cleaning temperature $\approx$1050 °C and doping concentration $N_D \lesssim 1\times 10^{15}$ cm$^{-3}$ (HT-LD)

Under the HT-LD conditions, very different electrical transport behavior was observed from the LT case. The apparent SBH from *I-V* measurement was found to be much higher than the usually reported value at LT for every silicide and metal tested. For instance, typical *I-V* traces for a few silicide phases are shown in Fig. 10, where the substrates had been cleaned at 1050 °C for 2 min. The increase of the apparent SBH was always accompanied by a high ideality factor ($\geq$1.2). Occasionally, a small component of recombinationlike current was observed. If the usual thermionic-emission equation and parameters were assumed, SBH's of over 0.75 eV were deduced for every silicide tested. Table III summarizes the apparent *I-V* SBH observed under HT-LD conditions. A comparison is also made with SBH obtained under LT, or the usually accepted SBH value for the silicide or metal. The observation of high SBH was independent of whether oxide pattern or plateau structure was used. High SBH ($>$0.75 eV) was also found for silicides on the (100) substrate with $N_D \approx 1\times 10^{15}$ cm$^{-3}$, and for as-deposited metal layers (Co or Ni). Although the magnitude of the *I-V* SBH fluctuated from run to run, the values for type *A*

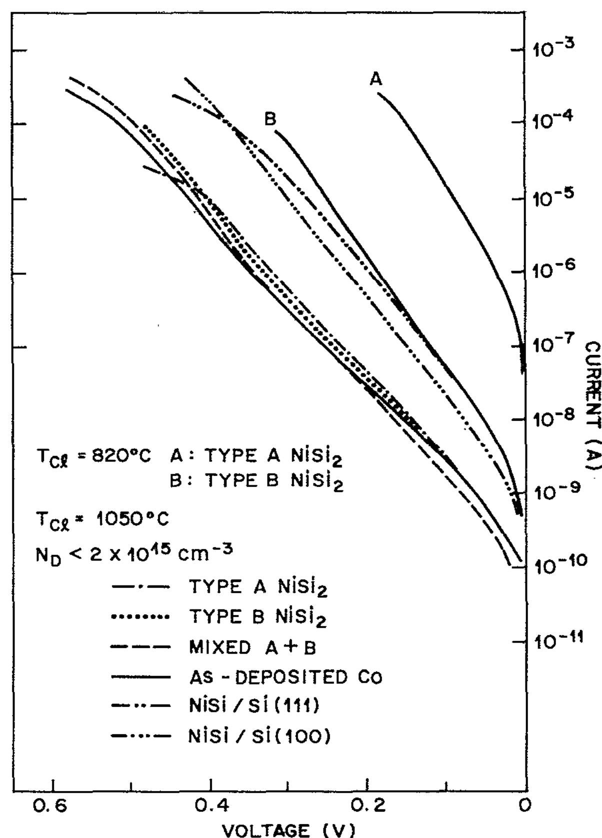


FIG. 10. *I-V* traces of an assortment of silicide-silicon junctions. All diodes have the same area, $\sim 2\times 10^{-3}$ cm$^{-3}$.

TABLE III. Effect of high substrate cleaning temperature and low substrate doping level on the apparent *I-V* Schottky-barrier height on *n*-type silicon. (poly denotes polycrystalline.)

| Silicide | Substrate | LT $\phi_{B0}^n$ (eV) | HT-LD $\phi_{B0}^n$ (eV) | HT-LD $n$ |
|---|---|---|---|---|
| Type-*A* $NiSi_2$ ~60–70 Å | (111) | 0.65 | 0.75–0.87 | 1.2–1.3 |
| Type-*B* $NiSi_2$ ~60–70 Å | (111) | 0.79 | 0.82–0.87 | 1.2–1.3 |
| Mixed *A* + *B* $NiSi_2$ ~70 Å | (111) | 0.66 | 0.85 | ~1.2 |
| Type-*A* $NiSi_2$ ~800 Å | (111) | 0.65 | 0.84 | ~1.2 |
| Type-*B* $NiSi_2$ ~800 Å | (111) | 0.79 | 0.83 | ~1.2 |
| $CoSi_2$ ~200 Å | (111) | 0.64 | 0.74 | ~1.2 |
| poly NiSi ~300 Å | (111) | 0.65[a] | 0.76 | 1.2 |
| poly NiSi ~300 Å | (100) | 0.68[a] | 0.77 | 1.25 |
| as-deposited Ni ~100 Å | (111) | 0.61[b] | 0.85 | 1.4 |
| as-deposited Co ~100 Å | (111) | 0.70[b] | 0.85 | 1.4 |

[a]Reference 11.
[b]Reference 15.

and type $B$ grown side by side in the same run were always close together (±0.02 eV). A few samples were obtained on substrates heated to 1050 °C for only 10—15 sec; high SBH's (>0.83 eV) were also observed for either type-$A$ or mixed $A+B$ $NiSi_2$ layers. Another property of the $I$-$V$ behaviors of HT-LD samples which differed from the LT case was their sensitivity to light illumination. A comparison is made in Fig. 11 of $I$-$V$ characteristics of a HT-LD sample with and without illumination.

The $1/C^2$ plots for the majority of the samples had considerable curvature. In the few samples where an approximate linear relationship was seen, extrapolation yielded high built-in potentials. Capacitances were found to be independent of frequency. The slopes were in reasonable agreement with the bulk doping levels. The built-in potential of a mixed-type $A+B$ layer on 9-Ω cm substrates heated to ~1050 °C for 10 sec was ~0.55 eV, implying a $\phi_{B0}^n$ of 0.86 eV (Fig. 12). For a 2-min heating period, the built-in potential was usually ~0.6—0.65 eV for type-$A$ $NiSi_2$ layers.

Layers of type-$A$ $NiSi_2$ and polycrystalline NiSi were grown on $p$-type Si(111) cleaned by heating to ~1050 °C for 2 min. The SBH's were determined from $I$-$V$ measurements at below room temperature to lie between 0.43—0.47 eV for both samples, in agreement with the LT results. So, the increase in the apparent SBH on $n$-type Si was not accompanied by a decrease in the SBH on $p$-type Si. This fact does not support a shift in the FL position at the silicide—$n$-type Si junction under HT conditions.

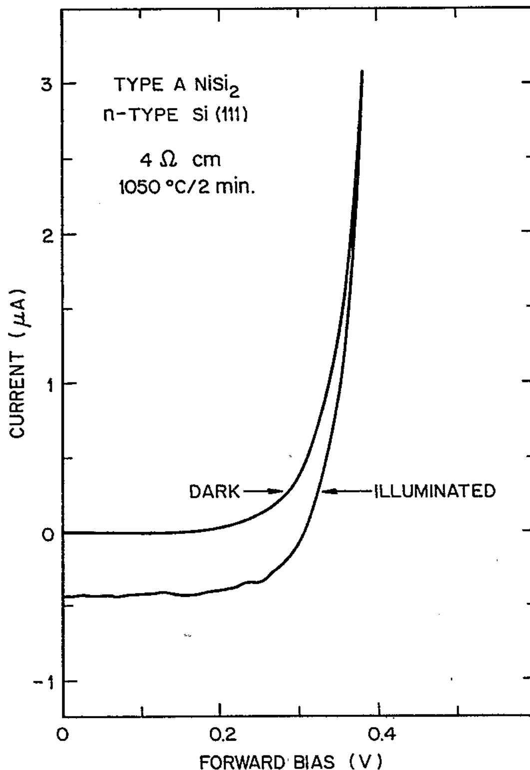


FIG. 11. $I$-$V$ curves of a type-$A$ $NiSi_2$ layer on a HT and LD substrate, with and without the illumination of a microscope lamp.

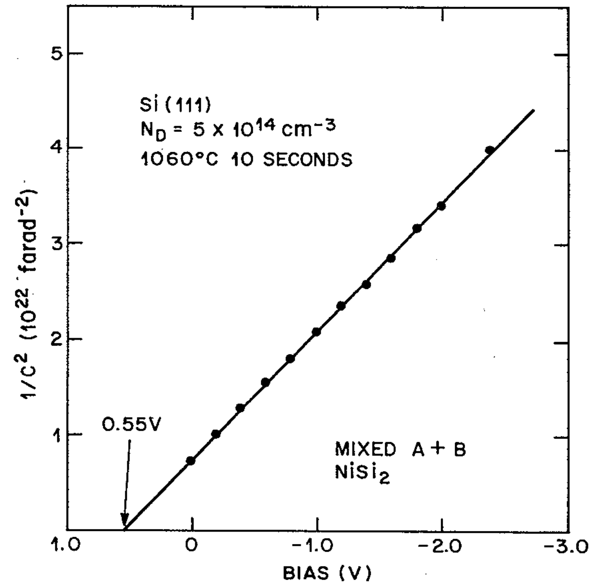


FIG. 12. $C$-$V$ plot of a mixed $A+B$ $NiSi_2$ layer under HT-LD conditions.

### C. Substrate-cleaning temperature ≈1050 °C and doping concentration $N_D \gtrsim 6\times10^{15}$ $cm^{-3}$ (HT-HD)

The $I$-$V$ behaviors under HT-HD conditions were almost identical to the LT case. The measured SBH took on the same values as the LT samples. However, $1/C^2$ plots of these samples had a distinctive bowing feature, indicative of a nonuniform doping profile. No determination of SBH was possible from $C$-$V$ due to this difficulty.

The HT-HD case is a transition region between the LT and the HT-LD cases. In the former, close to ideal SB behaviors were observed, and in the latter there seemed to be problems with interpretation of the data with a simple Schottky picture. In the intermediate region, ideal SB behaviors were observed from $I$-$V$ measurements. The capacitance study, on the other hand, suggested the presence of a nonuniform doping profile. The SBH's of type-$A$ $NiSi_2$ obtained from $I$-$V$ analyses are listed in Table IV as a function of $T_{cl}$ and $N_D$.

TABLE IV. Schottky-barrier height of type-$A$ $NiSi_2$ on $n$-type Si(111) from $I$-$V$ measurements.

| $N_D$ ($cm^{-3}$) | $\phi_B^n$ (eV) $T_{cl}=820$ °C | $\phi_B^n$ (eV) $T_{cl}=1050$ °C |
|---|---|---|
| $3\times10^{16}$ | 0.63 | 0.64 |
| $6\times10^{15}$ | 0.64 | 0.64 |
| $1\times10^{15}$ | 0.65 | ~0.83 |
| $5\times10^{14}$ | 0.65 | 0.80—0.87 |
| $2\times10^{14}$ | 0.65 | ~0.81 |

## IV. DISCUSSION

### A. Review of previous results

The main motivation behind the present study has been to understand the circumstances under which discrepancies might develop regarding SBH measurements of metal-semiconductor systems. The central issue involves the SBH's of single-crystal $NiSi_2$ on $n$-type Si(111), where Tung[8] found a high SBH (0.79 eV) for type $B$ and a low SBH for type $A$ (0.65 eV) and mixed $A+B$ (0.66 eV), while Liehr *et al.*[9] attempted to follow the silicide growth techniques described by Tung[4] and found a high SBH (0.78 eV) for both pure type $A$ and pure type $B$ and either a low (0.64 eV) or high (0.78 eV) SBH for the mixed $A+B$, depending on grain size. The difference is therefore the observation of high SBH for type-$A$ layers and, occasionally, for mixed $A+B$ layers by Liehr *et al.*[9] We will first review the experiments described in the two reports. Differences in the procedures are identified. Our present results are then discussed, aimed at resolving the controversy based on the identified differences.

Tung[8,11] had used deposition and reaction techniques which had repeatedly been shown by plan-view and cross-section TEM to produce pure single-crystal layers on Si wafers. The actual diodes, however, were grown in small windows surrounded by $SiO_2$. LEED and channeling were used to determine the orientation of the $NiSi_2$ layers grown as a control on large nearby Si areas on every sample. Results of these characterizations were identical in every respect to those from layers which had been checked by TEM to be of pure orientation. So the orientations of the $NiSi_2$ layers in Tung's study were very likely of pure orientation, but for the sake of argument, should be regarded as suspect. The fact that electrical measurements were performed on diodes inside oxide windows is the source for some other uncertainties. The problem rests with the possibility of contamination diffusing out of oxide and into the Si openings and hence affecting the interface impurity level, the interface roughness, and the silicide orientation.[9] In earlier experiments, Tung[8,11] had used a HF etch and methanol rinse which led to high carbon content on the starting surface. Later,[12] only the Shiraki method was used. After heating, no difference was seen in either the Si-surface cleanliness, the epitaxial characteristics, or the electrical results. So the difference in the cleanliness of the starting surface does not seem to be a prime factor.

The shortcomings of Tung's[8] original work have been eliminated in the present study by the use of Si without oxide patterning. TEM analyses of these layers ascertained the fact that these are single-crystal layers of high perfection. The electrical behavior of plateau structures was found to be identical to that of diodes formed inside oxide windows. This clearly demonstrated that patterned oxide had no effect on the characteristics of SBH.

Some details of Liehr *et al.*'s experimental conditions are not known to us, but potential problems can develop in a few areas according to the published procedures.[9] Cross-section TEM was used instead of conventional plan-view TEM to determine the silicide orientation. This is very time consuming, so only a few samples from each type were studied. A more serious problem is that only a very small area ($\sim 0.01\ \mu m^2$) on each sample can be imaged. This is worrisome because the average grain size for mixed $A+B$ films are often as large as 0.5 $\mu$m even for very thin layers[16] (< 100 Å). Liehr *et al.*[9] had correlated SBH's with the average grain sizes ($\sim 0.1\ \mu$m) of mixed $A+B$ layers. This correlation is suspicious because any grain-size estimation by cross-section TEM alone is known to be inherently unreliable. The main difficulty of Liehr *et al.*'s results, as we discovered, is with the substrate-cleaning temperature that was used. This effect will be described below in detail.

### B. The present study

Some of the differences in the experimental procedures adopted in the two laboratories and listed in Table I may have no effect on the SBH. However, variation of two parameters, $N_D$ and $T_{cl}$, resulted in a substantial variation in the apparent SBH. Under LT conditions, the present study reproduced Tung's results.[8,11] Near-ideal diode characteristics were observed, namely a long and straight linear relationship for $\log I$, and $1/C^2$ plots from $I$-$V$ and $C$-$V$ measurements and good ideality factors for $I$-$V$ traces. SBH's determined from $I$-$V$, $C$-$V$, and activation-energy studies are all in good agreement with each other. No dependence on substrate doping was observed. The SBH's on $p$-type SBH's complemented the $n$-type SBH's. These studies offered no evidence for any interpretation other than that the interface FL position for type $A$ is closer to the conduction-band edge by $\sim 0.14$ eV than for type $B$.

The HT data showed huge scatter. The overwhelming result was that on LD substrates the apparent $I$-$V$ SBH of every silicide metal phase tested was much greater than the SBH generally reported for that particular phase. Very poor diode characteristics were observed, namely poor $I$-$V$ ideality factors, curving $C$-$V$ plots, and the fact that these two different measurements did not agree on the magnitude of the SBH. However, upon the use of higher doping concentration (HD), these abnormalities disappeared and SBH's of LT conditions were recovered.

The experimental conditions of Liehr *et al.*[9] fall within our HT-LD category. The presence of a high apparent SBH for pure type $A$ and mixed $A+B$ $NiSi_2$ layers under HT-LD conditions appeared to agree with the results of Liehr *et al.*[9] These are, however, differences. Notably, we have not seen any $I$-$V$ SBH's below 0.75 eV under HT-LD conditions, while Liehr *et al.*[9] occasionally obtained $\sim 0.66$ eV for mixed $A+B$ layers and for contaminated silicides. Furthermore, the good ideality factors that Liehr *et al.* reported were never observed under our HT-LD conditions. Differences in heating time and temperature in these two studies may have contributed to these differences. Nevertheless, it is not yet absolutely certain that the high apparent SBH which we observed is caused by the same effect which allowed the observation of Liehr *et al.* of a high SBH. However, one important point is clearly demonstrated: the apparent SBH will vary appreciably depending on the two parameters $T_{cl}$ and $N_D$.

Tung[8] and Liehr *et al.*[9] happened to use choices of these two parameters which in the present study produced very different results. Therefore, this effect has to be considered and understood when SBH's are analyzed. The questions which then become important are "what is this effect which can change the apparent SBH" and "which set of experimental conditions gives more reliable SBH measurements?"

### C. The effect of HT and LD

The first thing we have to be concerned with is whether this apparent SBH increase represents a change in the FL position [see Fig. 13(a)]. This FL change could have arisen from a change in the interface-state density because higher cleaning temperature changes the impurity or defect concentration and/or changes the interface microstructure. This could either free the FL from the previous pinning mechanism or pin the FL to a new position. However, for reasons discussed below, a FL change can be ruled out. The main argument against a FL change is that this effect depends on doping concentration. No change in SBH was seen on substrates with $N_D > 6\times10^{15}$ $cm^{-3}$ and on *p*-type substrates, when HT was used. The interface morphology, structure, impurity concentration, etc. are not expected to change with doping, and states from shallow dopants are not known to influence the FL at these concentrations. Another reason not in favor of a FL change is the departure of the characteristics from ideal SB behavior. In itself, this nonideal behavior argues against a FL change. Finally, the phenomenon of surface *p*-type layer formation, known in the literature to occur under these conditions, is positively identified and is capable of explaining every piece of experimental data without invoking a FL change.

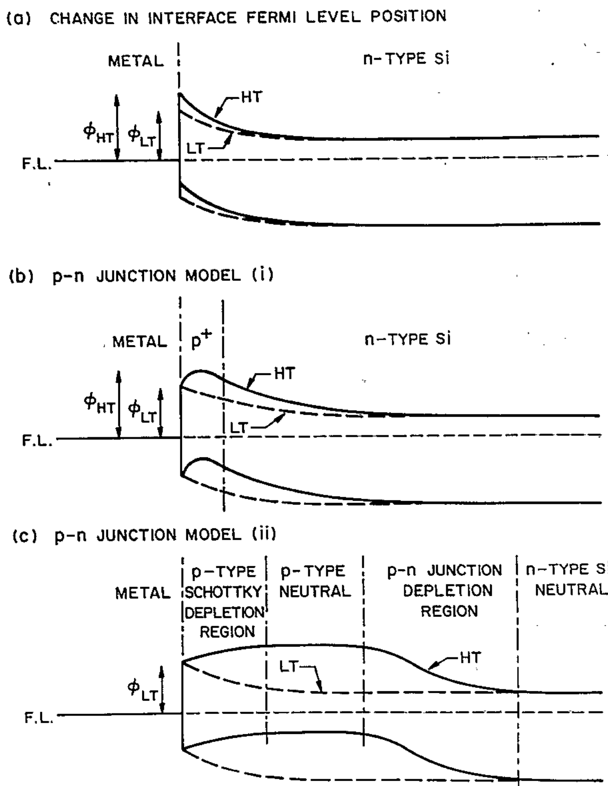


FIG. 13. Possible models of the band bending at a HT-LD interface for the increase of the apparent SBH.

If the FL position remains the same, what are the mechanisms which will yield a higher apparent *I-V* SBH? Trivial answers like discontinuous metal film, poor Ohmic contact, etc. can be ruled out. The only mechanism that we are aware of is the introduction of negative charge near the interface. Acceptors and charged traps near the interface can cause upward band bending and hence an apparent SBH increase.

There are two distinct stages of sample preparation at which defects and contaminants could be expected to diffuse into the bulk substrate. The first occurs during the thermal cleaning cycle, whereas the second takes place when the nickel overlayer is reacted with the substrate around 500 °C to form the disilicide. DLTS studies by Weber[18] indicate that the 3*d*-transition metals such as Ni form donors in Si. Nevertheless, resistivity and Hall measurements[19,20] show that *n*-type Si may be compensated, but in any event Ni is not the cause of the negative charge at the interface, because even for cobalt silicide and as-deposited Ni and Co the effect persisted.

Concerning the thermal cleaning in UHV, there exists considerable experimental evidence that this process produces acceptor-type defects,[21-26] which diffuse into *n*-type Si at temperatures in excess of 1000 °C. This seemed to be associated with resistive heating. The physical identity and the source of the acceptorlike trap have yet to be firmly established. However, we note that boron has been positively identified in a few studies,[22,25] and a correlation with surface carbon contamination has been suggested by others.[26] It is important to point out that, because we observed this effect with and without $SiO_2$, the patterned oxide is ruled out as the main source of contamination. The extent of the *p*-type layer is usually a few micrometers in depth with an average doping concentration of $\gtrsim 10^{15}$ $cm^{-3}$.[21] The temperatures used in these studies were usually greater than 1200 °C and long anneal times (> 15 min) were used. Near the reported onset temperature for the phenomenon, 1000 °C, less data are available. Because this is most probably due to an impurity effect, differences in ambients and sample handling among laboratories can lead to very different results. So clearly we need to determine for ourselves what the likely concentration and depth of impurities are.

### D. Determination of surface *p*-type doping concentration from SBH results

Two models can be distinguished based on the acceptor-to-donor ratio $N_A/N_D$ and the width $d$ of the acceptor profile. For simplicity the acceptor profile is assumed to be planar in the following discussion. The space-charge density and band-edge diagram associated with these two models are shown schematically in Fig. 13.

Model (i) is a metal-shallow $p^+$-$n$ structure where the *p*-type layer is fully depleted. Such structures have been deliberately fabricated and have been studied in detail in the literature.[27] Usually, $N_A \gg N_D$ and $d \ll W$ have been

used, where $W$ is the space-charge width in the absence of the acceptor doping. Assuming a planar acceptor profile and that the depletion approximation is valid, the SBH increase may then be solved analytically. However, such a structure has a light-sensitive barrier height[28] whose $I$-$V$ characteristic is shifted in a qualitatively different fashion from those of either a Schottky barrier or a $p$-$n$ junction. In Fig. 11 the $I$-$V$ characteristics of a HT-LD sample are shown with and without illumination. The turn-on voltage under illumination is not shifted toward lower positive bias as predicted by the band-edge diagram of model (i). This shift should be expected to occur because photoinduced holes generated by band-gap illumination which collect at the potential hump can lower the effective acceptor concentration. Another feature of model (i) which is inconsistent with our data is that the $B$-type barrier height should increase nearly as much as the $A$ type, thus maintaining a value always significantly higher than the observed SBH for type-$A$ $NiSi_2$. Because of these disagreements with experiment, model (i) is not favored as a realistic representation of the actual band bending.

Model (ii) represents the case of a $p$-$n$ junction in series with a $p$-type Schottky barrier [see Fig. 13(c)]. This model differs from model (i) in that it requires type conversion of the surface layer to a depth such that the space-charge regions of the $p$-$n$ junction and the Schottky barrier are separated by a neutral region. The extent of the HT-induced $p$-type surface layer reported in the literature[21,22,25] are in perfect agreement with the conditions of model (ii). We also find this model to be capable of explaining our experimental results. The SBH's recorded in Tables III and IV as a function of substrate-doping and substrate-cleaning temperature can now be explained as follows. For substrates typically doped to donor concentrations exceeding $6\times10^{15}$ cm$^{-3}$, there are insufficient acceptors generated during the 1050 °C cleaning cycle to convert the surface type, so that no $p$-$n$ junction forms. As a result, we have never observed a high $A$-type barrier on material doped at 0.6–$3\times10^{16}$ cm$^{-3}$.

On substrates with $N_D \leq 1\times10^{15}$ cm$^{-3}$, a 1050 °C anneal for 2 min converted the surface region to $p$ type. This puts the uncompensated acceptor concentration at $1\times10^{15} < N_A < 6\times10^{15}$ cm$^{-3}$ for such an anneal. The depth of this $p$-type layer is estimated to exceed 0.5 $\mu$m to make the apparent SBH independent of the original FL position. It should be stressed that these estimates were arrived at based on the results of many different runs, where fluctuations were inevitable and as such they should be regarded as order-of-magnitude estimates. Nevertheless, we note that these estimates are in good agreement with other reports in the literature.[21–26] In an $I$-$V$ measurement, since the voltage applied is shared between the $p$-$n$ junction and the $p$-type SB, a low current level is expected as well as a high ideality factor. Hence, the apparent $I$-$V$ SBH of every silicide metal junction was high. The $C$-$V$ measurements are consistent with the existence of a $p$-$n$ junction of doping levels of $\sim 10^{15}$ cm$^{-3}$. Such agreement is only qualitative due to the uncertainty with the exact doping profile. The same $p$-type formation may be expected on Si(100), explaining our observed result on that surface. On a $p$-type substrate, addition of acceptors do not convert the type and hence no change in the SBH was observed.

### E. Direct surface-doping profiling

Recently, spreading-resistance (SR) measurements were performed on an assortment of unmetallized Si substrates which had been prepared in either the LT or the HT condition in UHV. A surface $p$-type layer is unambiguously identified on the $n$-type HT-LD samples as shown in Fig. 14. On samples heated to 1050 °C for 2 min, the depth of this $p$-type layer is $\sim$0.6 $\mu$m. The location of the $p$-$n$ junction is shallower ($\sim$0.2 $\mu$m) for samples heated to 1050 °C for only 10 sec. The nominal $N_A$ of these surface $p$-type layers determined from SR measurements is somewhat above the range of $N_A$ as deduced from SBH measurements. This difference may be due to possible error associated with the SR technique,[29] particularly in the presence of a $p$-$n$ junction. In addition, slight variation in sample prepartion can also bring about a different level of impurity concentration near the surface. The depths of the $p$-type layers are consistent with a $\sqrt{t}$ dependence. This tends to support the theory that these acceptor dopants had diffused from the surface. The HT treatment also enriched the surface of the $p$-type doped substrates as one of the profiles in Fig. 15 illustrates. The net increase in $N_A$ near the surface was $\sim 5\times10^{15}$ cm$^{-3}$, in good agreement with that determined from SBH measurements.

In the case of Si substrates heated to 800 °C (LT) for 2 min in UHV, the carrier density near the surface remained essentially unchanged from the bulk-impurity concentration as shown in Fig. 15. Therefore, this LT treatment produces substrates which are most suitable for SBH measurements upon metallization. Under the HT-LD conditions, the surface-doping profile is quite com-

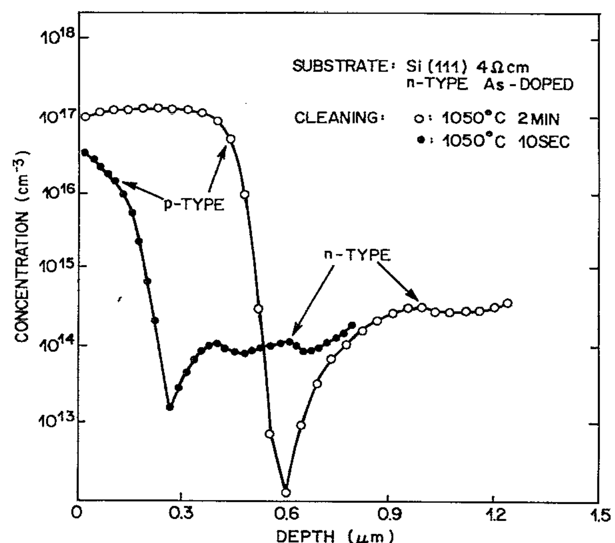


FIG. 14. Carrier-concentration profiles of Si(111) samples with $1\times10^{15}$ cm$^{-3}$ bulk-doping concentration. One sample has been cleaned by the Shiraki method and heated in UHV to 1050 °C for 2 min, the other has been degreased and heated to 1050 °C for 10 sec.

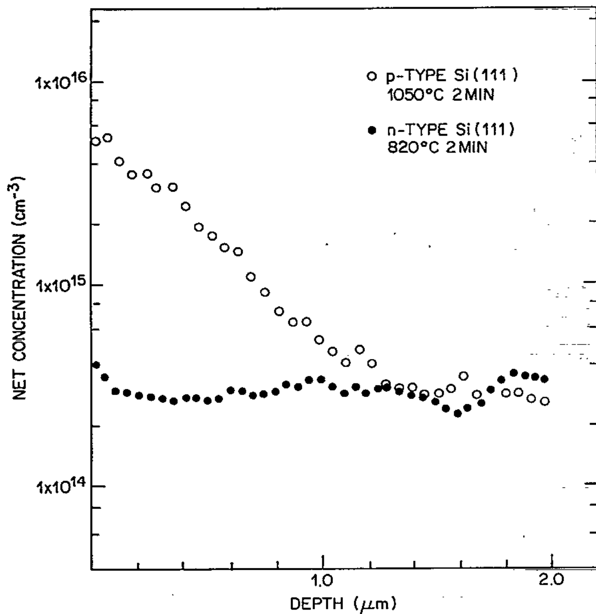


FIG. 15. Carrier-concentration profiles from spreading resistance measurements of a $p$-type Si(111) substrate heated to 1050 °C and an $n$-type Si(111) heated to 800 °C for 2 min.

plex. A $p$-$n$ junction forms after heating to 1050 °C for as short as 10 sec. Under this complicated band diagram [Fig. 13(c)], it is extremely difficult, if not impossible, to determine the metal-semiconductor interface FL position. Inaccurate conclusions can be drawn about the magnitude of the SBH from transport measurement through the entire structure, if a simple Schottky-barrier picture is assumed. For this reason, it is clear that we should absolutely avoid using the HT-LD conditions when performing SBH measurement, and that any SBH measurements carried out under the HT-LD conditions are likely to be fortuitous.

## V. CONCLUSIONS

The formation of a $p$-type layer on an $n$-type substrate at high annealing temperature is most likely due to impurities. The depth and carrier concentration of the $p$-type layer should depend on parameters such as the temperature and duration of heating, the substrate doping, wafer handling, cleanliness of the Ta or Mo clamps used in resistive heating, and other sources of impurities. The results in our laboratory seem to be consistent enough from run to run to observe a clear threshold of substrate-doping concentration where this effect is present. We expect when the HT annealing time is reduced, a less clear-cut situation may result. However, it was noted that heating to 1050 °C for as short as 10 sec already brought about a SBH increase of $\sim$200 meV on a substrate with $N_D = 5\times10^{14}$ cm$^{-3}$. These conditions are very similar to that employed by Liehr *et al.*[9]

All of our data obtained on substrates cleaned at $\sim$820 °C consistently indicated that the interfacial FL position for type-$A$ $NiSi_2$ is unshifted from the value of $\sim$0.65 eV. Conventional, plan-view TEM has shown these layers to be of essentially single orientation. Using experimental conditions similar to that of Liehr *et al.*,[9] we observed high apparent $I$-$V$ SBH for the type-$A$ layer, similar to that reported by Liehr *et al.* This increase was shown to be of spurious origin and not related to any change in the interface FL position. Rather, it is due to a thermally induced, type-conversion phenomenon near the surface which results in a $p$-$n$ junction in series with the Schottky barrier. Spreading-resistance measurements allowed direct observation of this $p$-$n$ junction. Because Liehr *et al.* happened to use experimental conditions[9] identical to those which produced spurious effects in our study, their results and conclusion must be viewed with suspicion. Under careful experimental conditions where no doping compensation occurs, the electrical behavior of the epitaxial $NiSi_2$-Si(111) interface is very consistent and well behaved. Tung's original results about the SBH's of type-$A$ and type-$B$ $NiSi_2$ are confirmed in this study. On $n$-type Si(111), the SBH of type-$B$ $NiSi_2$ is higher by $\sim$0.14 eV over the SBH for type-$A$ $NiSi_2$. Recent results[30] from other groups also agree with this dependence of SBH on the orientation of the silicide. This dependence is suggestive of an intrinsic mechanism for the Schottky-barrier formation.

There have been many recent calculations on the electronic structure of the epitaxial Ni-Si systems.[31–33] Unfortunately, the formidable task of performing a reliable calculation based on a realistic metal-semiconductor structure remains and any theoretical explanation of the difference between the SBH's of $A$- and $B$-type $NiSi_2$ is only speculative at this stage. Experimentally, the interfaces between single-crystal silicide and silicon remain the closest to ideal, simple, and well-controlled metal-semiconductor junctions available. The interface atomic structure of this system has already been studied in detail.[5–7] We expect much more work to be carried out in elucidating the electrical properties of these systems which, hopefully, can bring us to a better understanding of the SB-formation mechanism.

## ACKNOWLEDGMENTS

We are grateful to E. Kasper, M Liehr, G. P. Schwartz, A. Chantre, D. Hamann, and C. Clark for discussions.

[1] L. J. Brillson, Surf. Sci. Rep. **2**, 123 (1982).
[2] R. H. Williams, Contemp. Phys. **23**, 329 (1982).
[3] M. Schlüter, Thin Solid Films **93**, 3 (1982).
[4] R. T. Tung, J. M. Gibson, and J. M. Poate, Phys. Rev. Lett. **50**, 429 (1983).
[5] D. Cherns, G. R. Anstis, J. L. Hutchinson, and J. C. H. Spence, Philos. Mag. A **46**, 849 (1982).
[6] J. M. Gibson, R. T. Tung, and J. M. Poate, Mater. Res. Soc. Symp. Proc. **14**, 395 (1983).
[7] E. J. van Loenen, J. W. M. Frenken, J. F. van der Veen, and S. Valeri, Phys. Rev. Lett. **54**, 827 (1985).
[8] R. T. Tung, Phys. Rev. Lett. **52**, 461 (1984).

[9]M. Liehr, P. E. Schmidt, F. K. LeGoues, and P. S. Ho, Phys. Rev. Lett. **54**, 2139 (1985).
[10]A. Ishizaka, K. Nakagawa, and Y. Shiraki, in *Collected papers of the 2nd International Symposium on Molecular Beam Epitaxy and Related Clean Surface Techniques* (Japan Society of Applied Physics, Tokyo, 1982), p. 183.
[11]R. T. Tung, J. Vac. Sci. Technol. B **2**, 465 (1984).
[12]R. T. Tung and J. M. Gibson, J. Vac. Sci. Technol. A **3**, 987 (1985).
[13]R. T. Tung, J. M. Gibson, and J. M. Poate, Appl. Phys. Lett. **42**, 888 (1983).
[14]E. H. Rhoderick, *Metal-Semiconductor Contacts* (Clarendon, New York, 1978).
[15]S. M. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, New York, 1981).
[16]J. M. Gibson, R. T. Tung, C. A. Pimentel, and D. C. Joy, in *Microscopy of Semiconducting Materials,* edited by A. G. Cullis and D. B. Holt (Adam Hilger Ltd., Bristol, 1985), p. 173.
[17]A. Chantre, A. F. J. Levi, and R. T. Tung (unpublished).
[18]E. R. Weber, Appl. Phys. A **30**, 1 (1983).
[19]M. Yoshida and K. Saito, Jpn. J. Appl. Phys. **6**, 573 (1967).
[20]S. K. Ghandi and F. L. Thiel, Proc. IEEE **57**, 1484 (1969).
[21]J. D. Mottram, A. Thanailakis, and D. C. Northrop, J. Phys. D **8**, 1316 (1975).
[22]F. G. Allen, T. M. Buck, and J. T. Law, J. Appl. Phys. **31**, 979 (1960).
[23]L. N. Aleksandrov, R. N. Lovyagin, P. A. Simonov, and I. S. Bzinkovskaya, Phys. Status Solidi A **45**, 521 (1978).
[24]B. I. Boltaks and S. I. Budarina, Fiz. Tverd. Tela (Leningrad) **11**, 418 (1969) [Sov. Phys.—Solid State **11**, 330-333 (1969)].
[25]L. N. Safronov, L. N. Aleksandrov, and R. N. Lovyagin, Phys. Status Solidi B **107**, 461 (1981).
[26]H. Froitzheim, U. Köhler, and H. Lammering, Phys. Rev. B **30**, 5771 (1984).
[27]J. M. Shannon, Solid-State Electron. **19**, 537 (1976).
[28]G. Lubberts, B. C. Burkey, H. K. Bücher, and E. L. Wolf, J. Appl. Phys. **45**, 2180 (1974).
[29]J. Ehrstein, in *Non Destructive Evaluation of Semiconductor Materials and Devices,* edited by J. Zemel (Plenum, New York, 1978).
[30]R. J. Hauenstein, T. E. Schlesinger, T. C. McGill, B. D. Hunt, and L. J. Schowalter, Appl. Phys. Lett. **47**, 853 (1985).
[31]D. R. Hamann and L. F. Mattheiss, Phys. Rev. Lett. **54**, 2517 (1985).
[32]O. Bisi, L. W. Chiao, and K. N. Tu, Phys. Rev. B **30**, 4664 (1984).
[33]H. Lim and R. E. Allen, J. Vac. Sci. Technol. B **3**, 1221 (1985).