3.3 GHz SENSE-AMPLIFIER in 0.18 μm CMOS TECHNOLOGY

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ABSTRACT

The performance of a novel current-steering logic sense-amplifier (CSL-SA) is verified through measurements in 0.18 μm CMOS by implementing a CSL-SA flip-flop (CSL-SAFF). The measured operating frequency of 3.3 GHz in 0.18 μm is the highest performance results published to date in any CMOS technology. Measurements using 0.5, 0.35, 0.25 and 0.18 μm technologies show power and speed scaling of the new SA and SAFF to smaller geometries. The CSL-SA has better input sensitivity and 92% less clock-load compared to conventional voltage SAs.

1. INTRODUCTION

Flip-flops are an integral part of digital design because of their use in retime, deskew and receive circuitry. Previous work on flip-flops has included efforts at utilizing sense-amplifier front-ends to improve sensitivity and speed of conventional flip-flops [1]. The basic SAFF circuit contains a SA front-end followed by a latch stage.

Previous work on high-performance SAFFs has concentrated on improving the latch stage and has mostly ignored the sense-amplifier front-end. The SAFF reported in [1] uses a NAND set reset (SR) latch, [2] uses a hybrid-latch flip-flop, a semi-dynamic flip-flop in [3] uses dynamic-style FF, [4] uses a cross-coupled inverter latch, and [5] uses a N-C^{2}MOS latch. Common to all these designs is a standard sense-amplifier front-end. The sense-amplifier used in [1]-[5] will be called a conventional voltage mode sense-amplifier (CVSA) in this paper. The CVSA is designed for zero static power consumption and carries a high clock-load burden that limits its frequency scaling. The experimental results for CVSA designs have been limited to sub-GHz operating frequencies [4].

To use SAs in high-speed designs, they should be able to achieve a multi-GHz operating frequency without compromising the power, sensitivity and clock-load. The new SAFF implemented in this work uses current-steering logic (CSL) to improve the performance of the sense-amplifier and the latch stage. Compared to CVSA, CSL-SA has better input sensitivity and considerably less clock-load at higher-clock frequencies while achieving comparable power consumption (~10× less clock-load at 3.0 GHz).

A CSL-SA in 0.18 μm CMOS with a 4.0 fF clock-load was experimentally verified to operate at 3.3 GHz by implementing a CSL-SAFF. At 3.3 GHz the CSL-SAFF consumed 1.5 mW. The input sensitivity of the SA was better than 50 mV_{PP} at a bit error ratio (BER) < 10^{-11} for a 2^{31}-1 non-return to zero (NRZ) pseudo-random bit stream (PRBS). These are the highest performance results published to date in any CMOS technology. Design and test of CSL-SAFF in 0.5, 0.35, 0.25 and 0.18 μm CMOS show that the design scales well with decreasing minimum feature size.

Section 2 describes the operation of conventional voltage SA (CVSA) designs. Section 3 gives the circuit description and operation of the new sense-amplifier and flip-flop. Section 4 documents the experimental results.

2. BACKGROUND AND PREVIOUS WORK

The operation of a sense-amplifier consists of a precharge/discharge phase and an evaluation phase. A conventional voltage-mode sense-amplifier (CVSA) schematic is shown in Figure 1. To eliminate DC power consumption, the sense-amplifier has a clocked transistor in the evaluation chain and the evaluation chain depth is 3. The operation of the SA has been previously published in [4].

Evaluation speed of the CVSA is proportional to the evaluation chain conductivity and is inversely proportional to the capacitance. The precharge speed of the CVSA is proportional to the precharge transistor conductivity and is inversely proportional to the capacitance. The capacitance of the CVSA is a function of the load capacitance, evaluation chain capacitance and precharge transistor capacitance.

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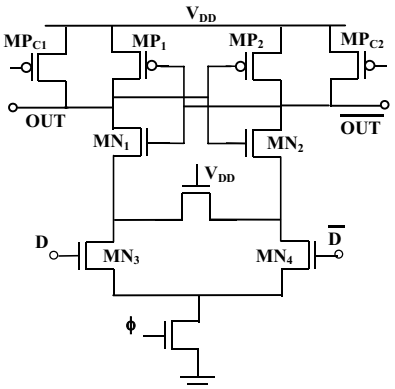

Figure 1 Conventional voltage sense-amplifier (CVSA).

For slower clock speeds, where the parasitic capacitance of the CVSA is smaller than the load capacitance, transistors can be resized to achieve better performance without significantly increasing the total output node capacitance. As a result, at slower clock speeds there is a linear relationship between the CVSA performance and the clock-load. A CVSA designed in 0.18μm CMOS technology optimized to operate at 1.0 GHz clock frequency has a clock-load that is 1.8× greater than a CVSA optimized for a 500 MHz clock frequency.

However, for frequencies above 1.0 GHz transistor resizing is of decreasing benefit. This is because the CVSA output parasitic capacitance is comparable to the load capacitance and resizing to improve CVSA performance also increases the total CVSA capacitance, limiting the overall performance improvement. At a clock frequency of 1.5 GHz CVSA output parasitic to load capacitance ratio is 0.75. If the transistors are resized by 2x the output node capacitance increases by 1.4x resulting in a 1.4x improvement in the speed. On the other hand, if the transistors are resized by 4x the resulting 2.3x increase in the output capacitance results in a 1.75x speed improvement. This analysis agrees with the Hspice simulation results given in Table 1. Compared to the 1.5 GHz CVSA, the 3.0 GHz CVSA achieved a 1.7x improvement in the evaluation delay at the cost of a 4x increase in the clock-load. Clearly the CVSA has serious performance limitations as clock frequency is increased.

Table 1: Hspice simulation results for a conventional voltage SAs (CVSA) optimized for different operating frequencies simulated in 0.18 μm CMOS. The output load is 10.0 fF and the target input sensitivity was 100 mV_{PP}.

Optimized operating frequency	Delay (ps)	Clock load (fF)	RMS Power (μW)
1.5 GHz	96	10	240
2.0 GHz	72	18	410
2.5 GHz	63	27	655
3.0 GHz	57	39	980

2. CURRENT-STEERING SENSE-AMPLIFIER FLIP-FLOP

The new SAFF discussed in this work replaces the CVSA with a current-steering logic sense-amplifier (CSL-SA) and latch stage is replaced with a clocked CSL NOR set-reset (SR) latch.

5.1. Sense-amplifier

The CSL-SA consists of a current-mode core and a differential input stage. The 3-deep evaluation chain of the CVSA is replaced in the CSL-SA current mode core with matched current sources. Removal of the clock transistor from the evaluation chain reduces the clock-load, improves the evaluation chain turn-on delay and has the added benefit of improved sense-amplifier noise and threshold variation tolerance. To further reduce the clock-load and SA output parasitic capacitance due to clocked transistors, the pMOS precharge of the CVSA is replaced with nMOS pre-discharge transistors, and the evaluation chain is changed from nMOS to pMOS. The improvement in the turn-on delay from static current sources, the 3× reduction in the evaluation chain depth, and reduced clock transistor parasitic allows us to size the pMOS current source transistor comparable to those of the CVSA cross-couple nMOS transistors without impacting the evaluation delay.

Figure 2 shows a schematic of the new CSL-SA portion of the design. When clock signal ϕ is high, both OUT and $\overline{OUT}$ are pre-discharged to ground. At the falling edge of ϕ, if node D is low, $I_d + I_s$ current flows through transistor MC_1 and only I_d current flows through MC_2. As a result of the current disparity, OUT changes from 0 to I_dR, while $\overline{OUT}$ remains at ground. When optimizing for higher frequencies, resistor R is eliminated to improve the frequency response, and current I_d is selected so that at the target frequency, transistors MP_1 and MP_2 are always in saturation ($V_{OUT} < V_b + |V_{thp}|$, where V_{thp} is the threshold voltage of the pMOS).

To improve the turn-on time of the evaluation transistors MN_1 and MN_2 and to reduce the clock-load, the pre-discharge transistor MC_1 and MC_2 width is selected so that during the pre-discharge phase the outputs remain just below V_{thn}. The transistor MC_3 is used for equalization of the output nodes during pre-discharge. In 0.18 μm CMOS technology, the CSL-SA with 50 mV_{PP} input sensitivity has an output delay of 500 ps and a power consumption of 870 μW at 3.3 GHz for an output load of 10.0 fF. The resulting power delay product of the CSL-SA of 44 fJ is 22% better even compared with a 3.0 GHz CVSA with 10.0 fF load and 100 mV_{PP} input sensitivity. A brief performance comparison of the two sense-amplifier architectures is given in Table 2.

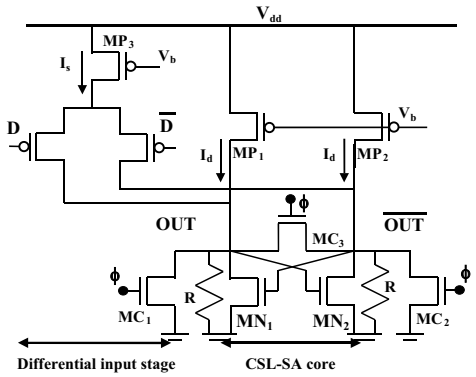

Figure 2 Schematic of the current-steering logic sense-amplifier. Differential inputs are D and $\overline{D}$. Differential outputs are OUT and $\overline{OUT}$, and clock is ϕ.

Table 2: Performance comparison between conventional voltage sense-amplifier (CVSA) and CSL-SA in 0.18 μm CMOS.

	CVSA	CSL-SA	Units
Operating speed	3.0	3.3	GHz
Input sensitivity	100	50	MV_{PP}
Output delay	57	50	ps
Clock-load	39	4	fF
Power consumption (RMS)	980	870	μW
Area	120	100	μm^2

5.2. SR Latch

The SAFF circuit consists of a sense-amplifier input stage and a CSL NOR SR latch output stage. A standard CSL SR latch and a clocked SR latch are shown in Figure 3. During clock high, both S and R nodes are at ground, and at the falling edge of the clock, one of the pre-discharged nodes is pulled up while the other remains at ground. A high (1) at S sets $\overline{OUT}$ to GND, which forces OUT to 1 (high). A high level of R sets OUT to GND, which forces $\overline{OUT}$ to 1 (high). As a result, there is a one-gate delay difference between the SAFF high-to-low transition and low-to-high transition. The delay difference between the high-to-low and the low-to-high can be 50 ps for a conventional CSL SR latch (17% of a 3.3 GHz clock period).

For a given input capacitance (input transistor size) the rise-time of the latch and delay difference can be improved by either increasing the size of the transistors MP_S or by reducing the size of the transistors MN_3 & MN_4. Both solutions increase the output low voltage of the latch stage. Additionally, increasing the MP_S transistor sizes without resizing the input transistor sizes appropriately can increase the fall-time and delay, which can offset any improvements in the output rise-time. Since increasing input transistor sizes increases the load at the SA, both the SA and the latch should be optimized together to achieve the best SAFF delay for a given output load and frequency.

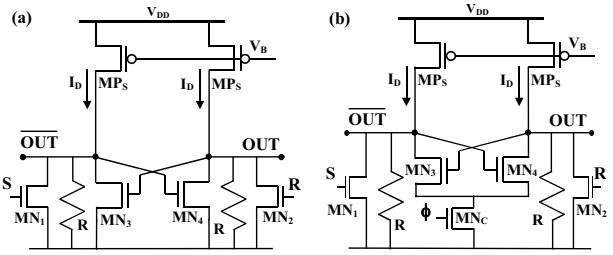

Figure 3 (a) Current-steering SR Latch (b) Clocked current-steering SR Latch.

To further improve the SAFF delay a clocked CSL-NOR SR latch is used. Due to the fast switching time of the CSL-SA (50 ps output delay at 3.3 GHz), the delay between the rise and fall outputs of the SAFF can be reduced by placing a clock transistor (MN_C) between transistors MN_3 and MN_4 (Figure 3.b). During the SA pre-discharge phase MN_C is on, and at clock low edge MN_C switches off allowing the high-going output to change without waiting for 1→ 0 transition at the complementary output. The MN_3, MN_4 and MN_C transistor sizes are selected such that they switch off only when the latch inputs have achieved $2 \cdot V_{thn}$. The addition of the clocked transistor MNC increases the total capacitance of the CSL-SAFF test circuit to 5 fF.

3. EXPERIMENTAL RESULTS

The die micrograph and the schematic of the SAFF test circuit are shown in Figure 4. On-chip 50 Ω terminations were included at the input and simple nMOS open-drain current-drivers were used at the output.

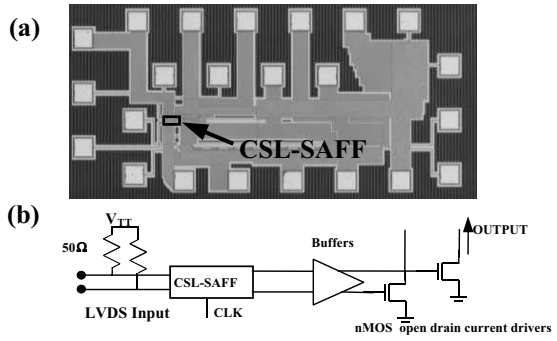

Figure 4 (a) Die micrograph of the CSL SAFF test chip in 0.18 μm CMOS with 75 × 75 μm^2 bond pads. The location of the CSL-SAFF circuit is indicated by the white box and has an area of 5 × 40 μm^2. (b) Test circuit schematic diagram

The input sensitivity and the output phase margin at 3.0 and 3.3 GHz are given in Figure 5.

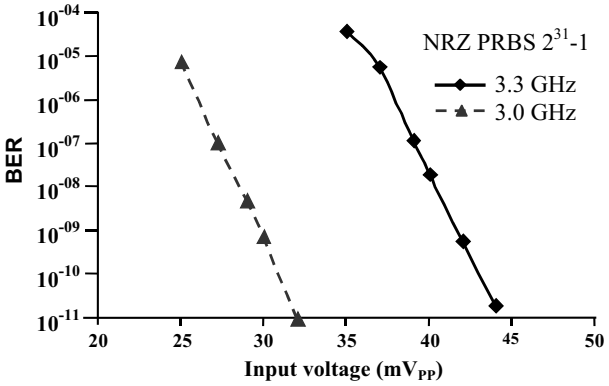

Figure 5 Measured input sensitivity of the SAFF at 3.0 and 3.3 GHz. Sensitivity is better than 35 mV_{PP} at 3.0 GHz (3.0 Gb/s) and better than 45 mV_{PP} at 3.3 GHz (3.3 Gb/s) for a 10^{-11} BER using NRZ PRBS 2^{31}-1.

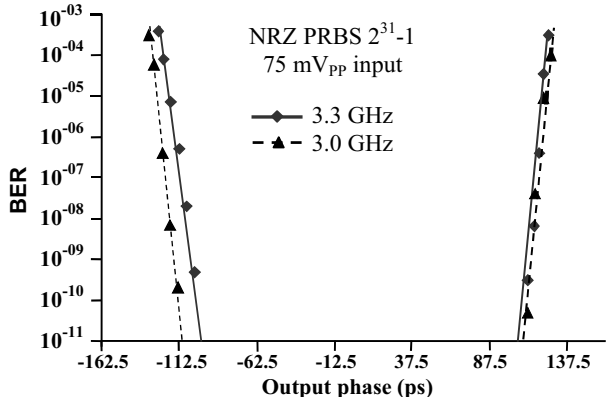

Figure 6 Output phase margin of the test circuit at 3.0 and 3.3 GHz clock frequency for a NRZ PRBS 2^{31}-1 input data pattern. The phase margin at 10^{-11} BER is 200 ps (66% of the bit period) at 3.3 GHz (3.3 Gb/s).

Table 3: Measured experimental results of the CSL-SAFF design in different technologies, shows power and speed scaling of the new design. As may be seen our CSL-SAFF in 0.18 μm CMOS operates at 3.3 GHz has a power consumption of 1.5 mW and an input sensitivity of 45 mV_{PP}.

Power supply V_{dd} (V)	3.6	3.3	2.5	1.8
CMOS technology (μm)	0.5	0.35	0.25	0.18
CSL-SAFF clock (GHz)	0.6	1.1	1.5	3.3
Measured sensitivity (mV_{PP}) BER = 10^{-11}, 2^{31}-1 NRZ PRBS	100	65	55	45
Power consumption (CSL-SA) (mW)	3.0	2.8	1.6	1.0
Power consumption (CSL-SAFF) (mW)	5.0	4.0	2.5	1.5

Table 3 compares the experimental results from the test circuits designed in 0.5, 0.35 and 0.25 μm CMOS technologies, indicating performance scaling of the CSL-SAs in deep sub-micron technologies. As seen in the table, with reducing feature sizes a better than linear improvement is seen in the CSL-SA operating frequency and a better than square improvement is seen in the speed-power-ratio.

4. CONCLUSION

A new CMOS SA is implemented using current-steering logic to improve the performance of sense-amplifier flip-flops. The new SA clock-to-output delay is 20% faster, the clock-load is 92% lower and the power-delay-product is 28% better than the conventional voltage sense-amplifier. Eliminating the clocked transistor from the evaluation phase, adopting a pre-discharge architecture and reducing the evaluation chain depth to one transistor by using current-steering logic in the SA achieved these enhancements. The operation of the SA and its scaling was verified through measurements in 0.5, 0.35, 0.25 and 0.18 μm CMOS technologies. The measured 3.3 GHz operating frequency in the 0.18 μm technology is the highest SA and SAFF performance results published to date in any CMOS technology. This circuit is a basic building block that has more applications in high-speed circuit design. One such application is a high-performance low-power pass-transistor logic crossbar switch. In this case the CSL-SAFF will be used as a demuxing receiver at the I/O interface and will also be used for retiming and swing restoration within the crossbar core.

11. REFERENCES

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