Chip Scan: 3D x-ray imaging of CMOS circuits

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***Abstract*— Non-destructive x-ray imaging of CMOS integrated circuits has potential applications to failure analysis, design validation, and quality control. We show that three-dimensional (3D) images from a ptychographic x-ray laminography microscope with zoom capability can be used to obtain topologically correct metal-layer interconnect information.**

Keywords—Coherent x-ray scattering; ptychographic x-ray laminography microscope; non-destructive reverse engineering of integrated circuits; CMOS circuit interconnect; 3D x-ray imaging of CMOS circuits; CMOS circuit metrology; Chip Scan

I. INTRODUCTION

Current research in state-of-the-art ptychographic x-ray laminography microscopy has application to 3D imaging of large-area integrated circuits [1]. In principle, billions of CMOS transistors and their metal interconnects can be imaged using this chip-scan technique. The method, which makes use of coherent x-rays, is non-destructive and so allows reinspection of areas of interest at different levels of resolution. Not only is this of potential interest for non-destructive reverse engineering of integrated circuits, metrology, identification of manufacturing defects and counterfeit products, but it also enables a path to a certified trust service to ensure integrated circuits are manufactured to customer design.

Here, we report on an initial experimental study to explore the feasibility of extracting topologically correct metal-interconnect layers from 3D x-ray images of contemporary CMOS chips. The images are obtained using a prototype ptychographic x-ray laminography microscope with zoom capability [1].

II. COMPLEXITY OF METAL INTERCONNECTS

Metal interconnects in integrated circuit manufacture is complex and hierarchical. Patterned metal layers and vias define electrical interconnect and key aspects of circuit function. It is, in effect, a static connectome. Typically, in today's commercially relevant circuits, metal layers closest to transistors fabricated on the silicon substrate are a few tens of nanometers thick and have the smallest lateral feature sizes. Circuits can be manufactured with many copper and other metal interconnect layers embedded in an insulating dielectric.

Figure 1 illustrates the complexity of interconnect in a CMOS integrated circuit. The figure shows a 3D x-ray image of a small portion of an Intel Pentium G3260 processor manufactured in a 22 nm FinFET technology [2].

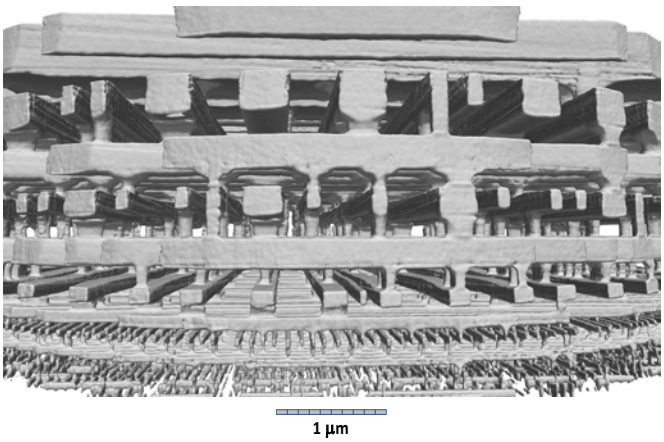

Figure 1: Example of metal interconnects in a CMOS circuit. The 3D-image created from coherent x-ray scattering data shows a small portion of an Intel Pentium G3260 processor manufactured in a 22 nm FinFET technology. Patterned metal layers connected by vias and metal interconnect closest to transistors fabricated on the silicon substrate have smallest lateral feature size.

Typical back-end-of-line fabrication processes use photolithography to define metal layers. The photolithographic masks that enable this are described using a standard GDS-II format. The masks contain the idealized circuit interconnect design information and can be mapped back to the circuit schematic. While actual manufacture of metal interconnects can deviate considerably from the intended design, the topology of the design must be respected to remain faithful to the circuit schematic.

A. Topologically correct extraction of manufactured metal layers

If the resolution and quality of the 3D x-ray image reconstruction is of sufficient fidelity, it is possible to create a topologically correct representation of a given manufactured metal layer by use of an optimized piecewise-constant cut through the image and appropriate image-processing.

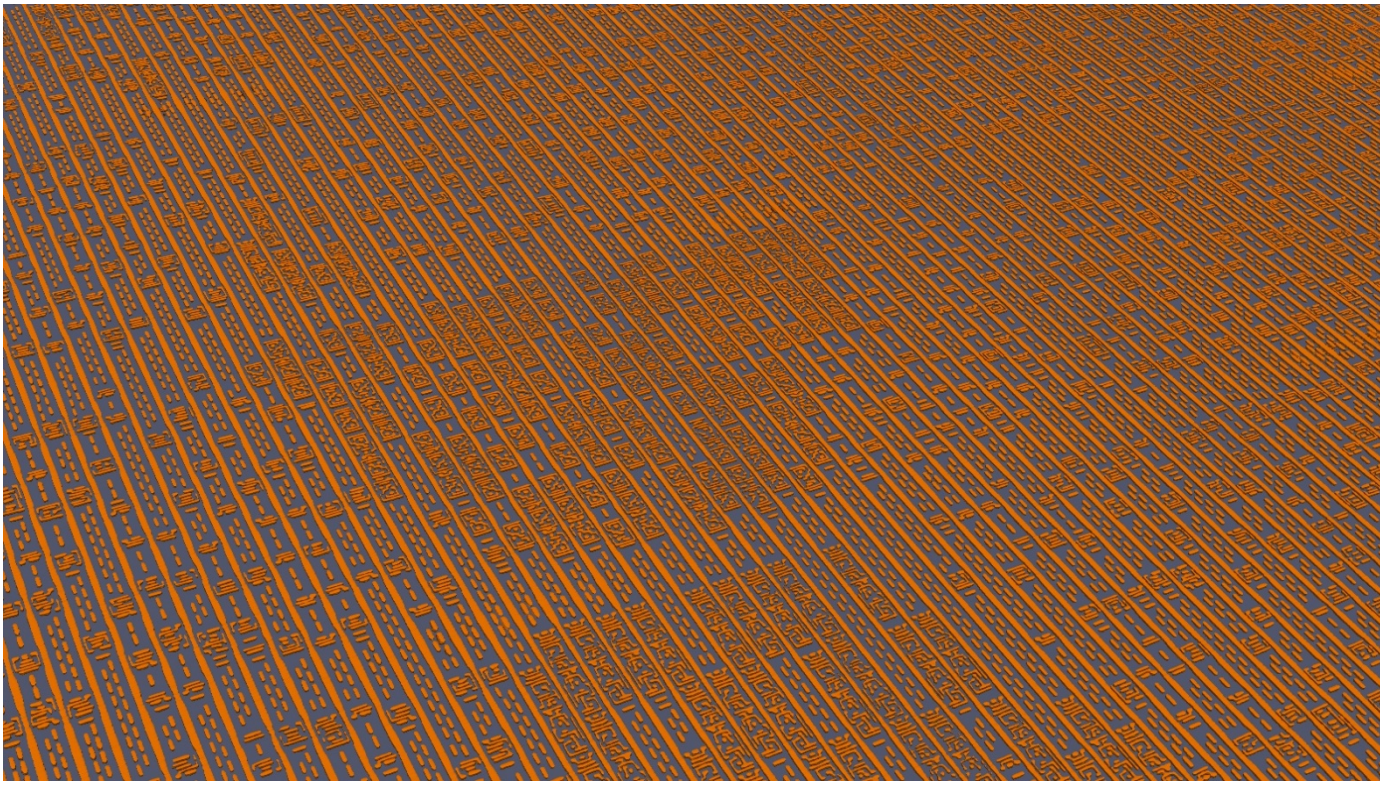

Figure 2: Example virtual delayered integrated circuit image obtained by ptychographic x-ray laminography microscopy. The 3D aerial-view image exposes metal interconnect layer M1 that is part of general-purpose logic circuitry implemented in a 16 nm CMOS FinFET technology. Pitch of the long metal lines is 576 nm.

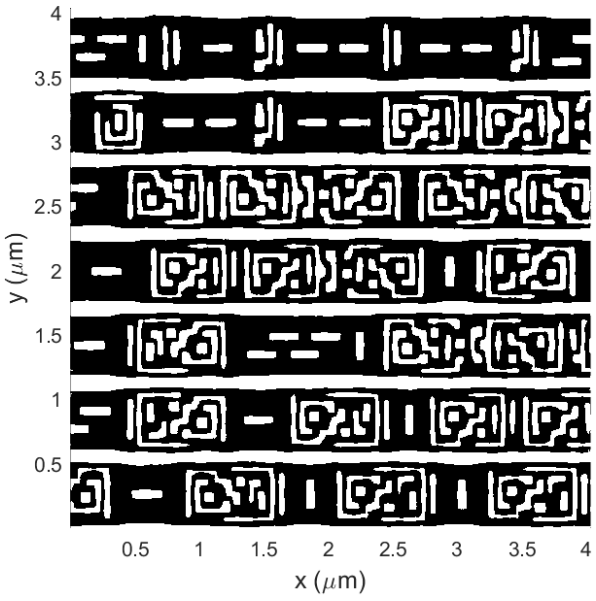

Figure 3: Thresholded image of horizontal cut through portion of the 3D M1 metal interconnect shown in figure 2. The connectivity of the metal layer is verified topologically correct by comparing with the GDS-II design.

Metal layers in a CMOS circuit design are usually numbered in ascending order of proximity to the silicon substrate. Processing a 3D x-ray image reconstruction of a circuit can be used to virtually delayer and expose each of these metal layers.

Figure 2 shows the result of virtual delayering an integrated circuit image obtained by ptychographic x-ray laminography microscopy. The 3D image exposes metal interconnect layer M1 that is part of general-purpose logic circuitry implemented in a 16 nm CMOS FinFET technology.

Figure 3 shows the result of applying machine-generated thresholding and image processing to a horizontal section through a portion of the 3D M1 metal-interconnect image shown in figure 2. In this case, the topology of the metal connectivity has been verified correct by comparing with the GDS-II design. The image processing that created figure 3 is an initial step in a method that converts a 3D x-ray image to 2D GDS-II design data and circuit schematics.

B. Identification of manufacturing errors

Identification of manufacturing errors can be achieved by comparing GDS-II design with measured x-ray images. To test this capability a small portion of the M1 layer is corrupted in the GDS-II design by substitution of a fake metal interconnect

pattern. Machine detection is then used to find the inconsistency in the measured x-ray data. An example of this automated detection is shown in figure 4. Both incorrect metal interconnect patterns of varying fill-density and complete absence of metal interconnect can be efficiently detected.

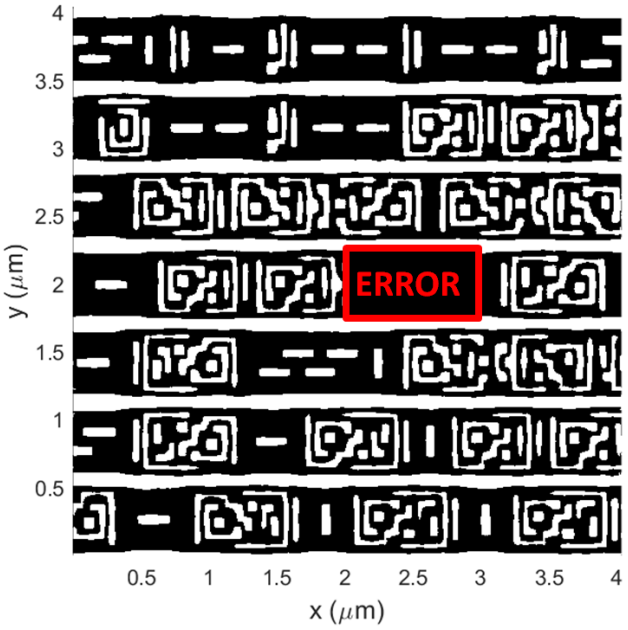

Figure 4: Automated detection of inconsistency between GDS-II design file for M1 metal layer interconnect and measured x-ray data. The size of the region containing the error region area is indicated.

III. Resolution and Scan Time

In principle, meaningful information about the integrity of integrated circuits manufactured in commercially relevant CMOS can be obtained in a few days by using x-ray chip-scan technology. No fundamental barrier has been identified that would preclude sub-2 nm resolution using the technique.

The ptychographic x-ray laminography microscope described in [1] has zoom capability so that any part of a chip up to 1.2 × 1.2 cm^2 in area can be examined with a selectable resolution. Overview scans can be performed without modification of microscope setup, and a region of interest for high-resolution 3D imaging can be studied as desired.

In initial proof-of-principle experiments, a low-resolution (500 nm) scan over a chip area of 300 × 300 μm^2 creating an image containing 2.3×10^7 voxels took 30 hours to acquire. A high-resolution (19 nm) sub-area 40 μm in diameter, in which 3800 × 3800 × 600 = 8.7×10^9 voxels with dimensions 13 × 13 × 13 nm^3 were created, took 60 hours to acquire.

In these first experiments the ptychographic x-ray laminography microscope was operated in transmission mode. Diffraction patterns were recorded for x-rays that had passed through the CMOS circuit and silicon substrate. The imaging rate, volume and resolution were limited by the available coherent x-ray flux. However, x-ray brilliance could be increased two orders of magnitude using methods pioneered by the Swedish MAXLAB [3]. An additional order of magnitude increase in flux can be obtained by increasing spectral bandwidth via use of multilayer mirrors [4]. A further order of magnitude increase in efficiency is available by replacing Fresnel zone plates with, for example, Kirkpatrick–Baez mirror systems [5]. Combining these improvements should increase total coherent flux by a factor of 10^4.

Scaling for ptychographic imaging [6] predicts resolution of 2 nm with the same measurement time as the initial high-resolution experiment, or inspection of an entire 1 × 1 mm^2 integrated circuit at 50 nm resolution in less than 30 hours.

Beyond higher flux, obtaining increased imaging speed and resolution can benefit from faster and more accurate sample scanning, improved x-ray probe stability and management of radiation damage. Upgraded mechanical and electronic hardware improves the imaging rate by decreasing imaging overhead [7]. Additionally, laminography reconstruction algorithms can exploit the sparse, laminar structure of ICs, as well as machine learned or prior knowledge from design files and fabrication processing, leading to measurements requiring fewer projections. For ptychographic reconstruction, some development is necessary and ongoing [8-10] to overcome the depth-of-field limitation on resolution, which is 12 nm for the results obtained in the initial experiments. Radiation damage can, in principle, limit achievable resolution. However, there is significant improvement in sample stability for laminography compared to tomography that uses isolated pillars. Small deformations that may occur during a measurement at higher dose can be accommodated within the reconstruction process [11].

IV. Metrology

In addition to measurement of critical dimensions, sidewall roughness, and other features obtained from 3D x-ray images of chips, it is possible to identify metals used in integrated circuit manufacture. For the 16 nm technology node this can include copper, aluminum, tungsten, and silicides.

Copper layers used as metal interconnects in contemporary CMOS circuits have microcrystaline structure, susceptibility to electro-migration and a barrier-metal encapsulation requirement that degrade electrical performance as layer thickness nears 10 nm. Such thin metal layers are needed to interconnect transistors with minimum feature sizes less than 5 nm and so alternative materials and approaches have been explored. Interconnect based on the rare transition-metal ruthenium is a promising candidate in part because of its high melting-point, chemical inertness, high bulk-conductivity, and potential for barrier-less implementation. Because of the metal thickness and small feature size, imaging with sub-10 nm resolution is required.

In the same ptychographic x-ray laminography microscope, x-ray fluorescence can be used to detect trace elements implanted for doping semiconductors. This capability has application to identification of transistor type as part of circuit schematic generation from x-ray imaging data.

Another potentially useful metrology is x-ray measurement of local micro-strain [12] that arises from the multilayer CMOS manufacturing process. Such measurements may be performed on unthinned chips.

V. Conclusion

A ptychographic x-ray laminography microscope with zoom capability can be used to non-destructively image metal interconnects in technologically relevant CMOS integrated circuits. Topologically correct 2D metal-interconnect layers can be automatically extracted from the 3D images obtained by reconstruction of coherent x-ray diffraction data. A machine-driven comparison between x-ray measurements of the manufactured chip and 2D GDS-II integrated circuit design information may then be used to detect fabrication errors. This represents an important first-step to certifying that chip manufacture is faithful to schematic design.

The chip-scan imaging capability described may be of interest for non-destructive reverse engineering of integrated circuits, metrology for advanced technology nodes, the efficient identification of manufacturing defects and counterfeit products, as well as enabling a path to a certified trust service that ensures integrated circuits are manufactured to customer design.

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