Summary Abstract: Hot-electron transport in the AlSb/InAs/GaSb double heterostructure prepared by molecular-beam epitaxy

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The concept of utilizing ballistic electron transport in transistor design to achieve high-speed operation has been proposed as early as 1960 by Mead. However, attempts to fabricate hot-electron transistor (HET) devices have not been fruitful because of stringent requirements in material processing technology. The interest declined until a decade later when Shannon was able to realize an HET structure in silicon by utilizing ion implantation to define abrupt *p–n* junctions. Using molecular-beam epitaxy (MBE), Malik *et al.* fabricated the first GaAs HET consisting of two planar doped emitter and collector barriers. AlGaAs barriers in GaAs HET design have also been realized later. However, the common emitter current gain of these early devices was generally unimpressive, even when operated at liquid helium temperatures. With the aid of hot-electron spectroscopy our understanding of nonequilibrium electron transport in semiconductors has improved.[1] For example, it is now known that the poor performance of GaAs HET's is due to a high hot-electron scattering rate for elastic and inelastic collisions with impurities and the plasmon/phonon system in the necessarily heavily doped transistor base. Consequently only a small fraction of the injected electrons transit the base ballistically, making GaAs an unsuitable material for the fabrication of high-performance HET.

The AlSb/InAs/GaSb double heterostructure HET's investigated in the present work have a number of advantages compared to the HET made from AlGaAs material system. The AlSb/InAs emitter/base heterojunction has a large conduction band discontinuity of 1.3 eV providing an injection energy more than 50 times greater than ambient thermal energies of $k_B T \sim 0.025$ eV at room temperature. Reverse current flows at both emitter/base and base/collector junctions are also minimized due to large barrier heights (typically we require >0.5 eV) compared to ambient thermal energy. Calculations indicate that, for a given resistivity of ambient carriers, scattering rates in bulk InAs are almost a factor of 2 less than in GaAs. In a HET device using a thin base width, scattering rates can be reduced further because the quantized two-dimensional electron states impose kinematic constraints on possible scattering processes. In a unipolar configuration the base resistance is low due to the high mobility of electrons in InAs and the forward bias emitter/base capacitance is low due to the absence of minority carrier diffusion. Hence this *RC* time constant, which limits bipolar transistor speed is unimportant, thereby allowing the unipolar HET to take full advantage of ballistic electron transport for high-speed operation.

The AlSb/InAs/GaSb system presents a number of difficulties from the materials point of view. A relatively large mismatch of 1.3% for AlSb/InAs and 0.62% for GaSb/InAs interface may lead to significant dislocation density in the device. Adding a small amount of As to the (Al,Ga) Sb layer may remedy this lattice mismatch problem but at the cost of additional complication of growing metastable alloy due to the existence of miscibility gap. These three binary material systems have different optimal growth temperatures. For MBE the use of different group V flux to stabilize the growth of such heterostructures creates difficulty in obtaining an abrupt heterointerface. Since the abrupt transition from one group V overpressure to the other is difficult using mechanical shutter in an MBE system, the coexistence of both species in the growth front of InAs or (Al,Ga) Sb may cause the exchange of As and Sb at the interface leading to localized compositional fluctuations or even worse three-dimensional growth at the interface. The lack of a lattice-matched semi-insulating substrate and difficulties in the processing technology of this material system require novel ideas and research efforts to overcome these problems. For the present work a growth temperature of 560 °C for (Al,Ga)Sb and 500 °C for InAs was used. The HET structure consists of a 1500 Å AlSb emitter, a 100 Å InAs base and a 3500 Å GaSb collector arm grown on (001)n^+ GaSb substrate. Although the thin base region is elastically strained, the thick AlSb layer has a tendency to relax giving rise to dislocations which can in principle be removed by growing lattice-matched AlSbAs. Abrupt interfaces are characterized by the immediate transition of the reflection high-energy electron diffraction pattern from (1×1) for InAs to (1×3) for (Al,Ga)Sb, and vice versa, without any three-dimensional nucleation stage during the growth. Dimeric As and Sb molecular beams improve the incorporation of group V elements and help to reduce the background As and Sb partial pressure.

To study the electron transport, the wafer is processed into a two-level mesa structure, then Ohmic contacts are evaporated for contacting each layer. Figure 1 shows the *I–V* characteristics measured at room temperature for the GaSb/InAs and AlSb/InAs heterojunctions, with an ideality factor of 1.14 and 1.4, respectively. A barrier height ~ 0.6 eV is obtained for the GaSb/InAs junction. For the AlSb/InAs junction the leakage current of $<10^{-7}$ A is improved by an order of magnitude compared to previous results.[2] Further reduction may require lattice matched growth of AlSbAs. From Shubnikov–de Hass measurement a two-dimensional electron density of $n \sim 2\times10^{12}$ cm^{-2} with a low-temperature mobility approaching 100 000 cm^2/V s has been obtained. The transistor characteristics measured at 300 K are shown in Fig. 2. The common emitter gain increases from $\beta = 10$ at collector/emitter bias voltage $V_{ce} = 1.0$ V to $\beta = 17$ at $V_{ce} = 3.0$ V, demonstrating the first room tem-

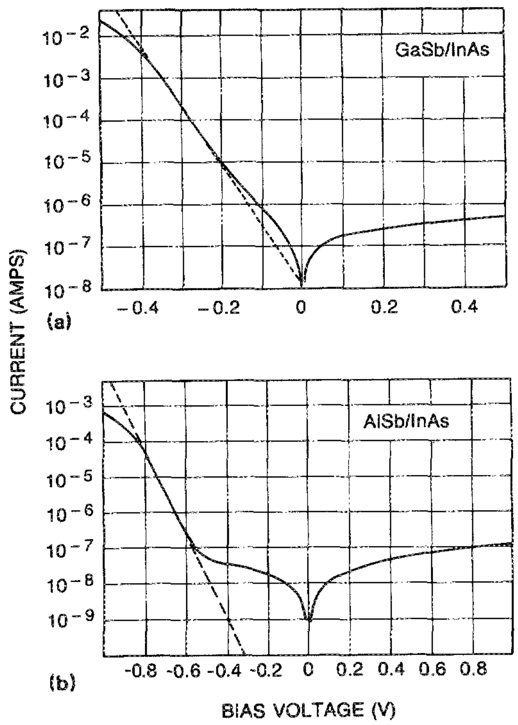

FIG. 1. Current–voltage characteristics of the (a) GaSb/InAs (active area is 2.0×10^{-4} cm^{-2}) and (b) AlSb/InAs (active area is 7.8×10^{-5} cm^{-2}) heterojunctions measured at room temperature.

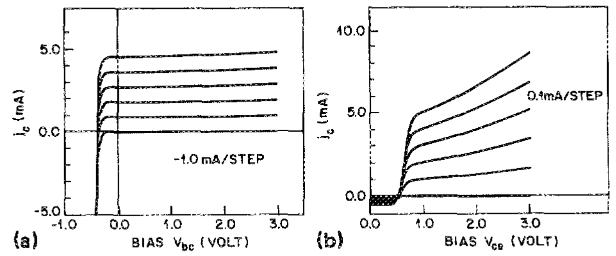

FIG. 2. (a) Room temperature common base current gain characteristics. Curves were taken in steps of − 0.1 mA starting with zero emitter injection current. (b) Room temperature common emitter current gain characteristics. Curves were taken in steps of 0.1 mA beginning with zero injected base current. Emitter area is 7.8×10^{-5} cm^{-2}.

perature operation of a unipolar HET with high-current gain.[3] In order to determine the true current gain of this device electron–hole pair generation by hot electrons in the collector must be avoided. Using a bias voltage $V_{ce} = 1.0$ V, for which the impact ionization is unimportant, we have measured $\beta = 10$ for collector current densities from 10 to 1200 A cm^{-2}.

The same double heterostructure has also been grown on GaAs substrates (using a 1 μm GaSb buffer layer) to study the effect of lattice mismatch on device performance. Preliminary results are encouraging. At room temperature a current gain $\beta = 10$ was measured for $V_{ce} = 1.0$ V, indicating that the presence of dislocations does not significantly affect the performance of this majority carrier device. However, the base/collector junction showed significant reverse bias leakage current ($\sim 50\,\mu$A at $V_{bc} = 1.0$ V). To improve this it will be necessary to reduce the dislocation density in the collector region.

For optimum device performance the quantum reflection of hot electrons from the base/collector barrier should also be minimized. This can be achieved by matching the hot-electron velocities on both sides of the heterojunction.[3] We note that the AlGaInAsSb alloy system lattice matched to GaSb offers a wide range of tunability of energy gap and effective electron mass in the collector for this purpose.

[1]For a review, and reference to earlier HET work, see J. R. Hayes and A. F. J. Levi, IEEE J. Quantum Electron. **22**, 1744 (1986).
[2]T. H. Chiu, W. T. Tsang, and A. F. J. Levi, Electron. Lett. **23**, 917 (1987).
[3]A. F. J. Levi and T. H. Chiu, Appl. Phys. Lett. **51**, 984 (1987).