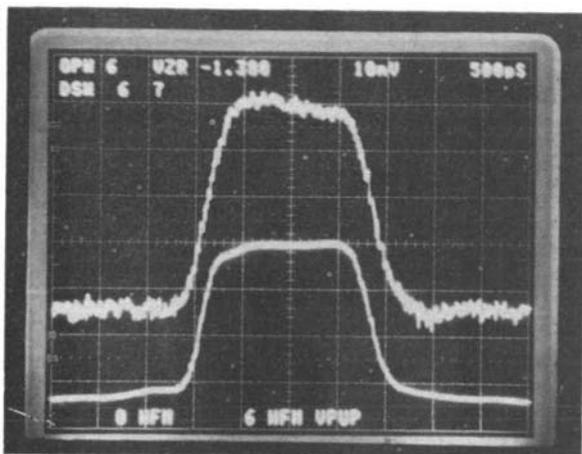


viously reported SEED arrays has been limited to $\sim 2\mu\text{s}$ by the limited forward current of the built-in tunnel junction.⁵ Fig. 3 shows the pulse response of one of the modulators in the 2×2 SLM. Rise and fall times of approximately 400 ps are observed. We believe this speed is limited by the speed of the electrical pulser generator, the RC time constant of the device and the inductance of the SLM mount. These speeds are far higher than those attainable with most other SLM technologies, which vary typically from tens of nanoseconds to hundreds of milliseconds.¹

We also studied the operation of this device at high optical power levels. For up to $\sim 400\mu\text{W}$ incident on an individual device the transmission/voltage characteristic and speed of response are basically identical to the data of Figs. 2 and 3. However, at approximately 1.1 mW input we saw a shift in the voltage of minimum transmission to lower voltage, along with a tail on the low-speed pulse response of approximately 1 ms duration. However, even at this power level the device showed a high-speed response essentially identical to that of Fig. 3. These data are consistent with a temperature rise of $\sim 10^\circ\text{C}$ as a result of optical power absorption. Improved heat-sinking of the array would presumably increase the power level below which heating effects are negligible.



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Fig. 3 High-speed pulse response of device 4

Lower trace is electrical drive pulse; upper trace is detected optical pulse. Horizontal scale is 500 ps/div. Rise and fall times of electrical pulse were 330 and 410 ps; rise and fall times of detected optical pulse were 390 and 460 ps. Data taken with same optical power and wavelength as data of Fig. 2

In summary, we have demonstrated a 2×2 array of individually driven MQW modulators which can be used for a variety of optical information processing applications. The devices show good uniformity in their transmission/voltage characteristics and useful values of contrast, insertion loss and drive voltage. The speed of response is much higher than that available in competing SLM technologies, and the crosstalk between devices is quite low. Further work should yield larger-scale arrays, perhaps utilising integrated electronic components¹⁰ for address control.

We wish to thank J. Centanni and R. Tucker for assistance with this experiment.

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ELECTRON TRANSPORT OF (Al, Ga)Sb/InAs HETEROJUNCTIONS PREPARED BY MOLECULAR BEAM EPITAXY

Indexing terms: Semiconductor devices and materials, Electron devices

Molecular beam epitaxial growth of (Al, Ga)Sb/InAs heterostructures is described. Electron transport studies indicate that these heterostructures are of high quality. Shubnikov-de Haas measurement of the AlSb/InAs/GaSb quantum well shows a two-dimensional electron gas of concentration $2 \times 10^{12} \text{ cm}^{-2}$ and a low-temperature mobility approaching $10^5 \text{ cm}^2/\text{Vs}$. Low-temperature capacitance/voltage measurement indicates that the thin AlSb barrier is a classical Mott-type barrier.

The concept of using ballistic electrons¹ to achieve high-speed unipolar transistor operation proposed in the early 1960s has encountered severe material problems for decades. With the continuing advance in the semiconductor epitaxial growth and processing technology, the hot-electron transistor concept has been realised in recent years in the Si^2 and GaAs/AlGaAs^{3,4} material systems. In addition to their potential high-speed device applications, hot-electron transistors also provide a unique opportunity to study the physics of hot-electron transport in semiconductors. With the invention of hot-electron spectroscopy,⁵ information about hot-electron momentum distributions can be directly accessed, providing a testing ground for the theory of nonequilibrium electron transport. Unfortunately, both theoretical and experimental results led to the conclusion that GaAs is not a suitable material⁶ for the fabrication of a useful, high-performance hot-electron transistor, because of an unacceptably short mean free path for hot electrons in the base region. InAs is a more suitable material for the transistor base because of its smaller effective electron mass and much reduced hot-electron scattering rate compared to GaAs.⁶ Furthermore, it can be closely lattice-matched to wider-bandgap materials such as the

AlGaInAsSb alloy system, providing a large electron injection energy compared to the ambient thermal energy. This is important for room-temperature operation. With this in mind, we have investigated the growth of (Al, Ga)Sb/InAs heterostructures on GaSb substrates by molecular beam epitaxy (MBE) and studied the heterojunction transport properties.

The epitaxial layer structure shown in Fig. 1a was grown in an MBE system on (001)-oriented Te-doped GaSb substrates. The antimony and arsenic tetramers were thermally cracked into Sb₂ and As₂ dimers by the high-temperature zone of the ovens to improve the incorporation efficiency of group V elements. The GaSb and the AlSb layers were grown at a temperature of 560°C, determined by an optical pyrometer. For InAs, however, a lower growth temperature of 500°C was necessary in the present growth configuration to minimise the exchange of Sb and As species at the heterointerfaces in the growth front, important for obtaining high-quality interfaces. Reflection high-energy electron diffraction (RHEED) was used to monitor the transition at each heterointerface. Abrupt interfaces were characterised by the immediate transition of the reconstruction pattern from (1 × 1) for InAs to (1 × 3) for (Al, Ga)Sb, and vice versa, without any three-dimensional nucleation stage. The thickness of the strained InAs layer was kept below 200 Å, ensuring commensurate growth. For the 1500 Å AlSb region there was a tendency to develop some dislocations, which could be removed with the addition of some As to improve the lattice-matching. The as-grown wafer showed excellent specular morphology under Normarsky microscopy.

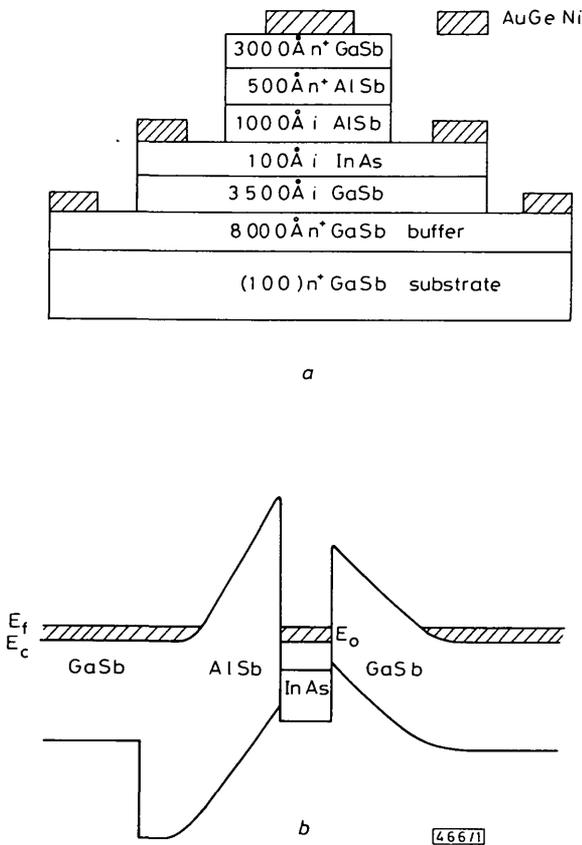


Fig. 1
 a Schematic diagram of epitaxial layer sequence and two-level transistor mesa structure for electrical measurements. Emitter area (AlSb) is $7.8 \times 10^{-5} \text{ cm}^2$ and base area (InAs) is $2.0 \times 10^{-4} \text{ cm}^2$
 b Band diagram associated with layer configuration in (a)

The unintentionally doped GaSb and AlSb epilayers show p-type conduction, and InAs n-type. Fig. 1b shows the schematic energy band diagram of our test structure using a 100 Å-thick InAs layer. From Shubnikov-de Haas measurement, a two-dimensional electron density of $n \sim 2 \times 10^{12} \text{ cm}^{-2}$ with a low-temperature (2K) electron mobility approaching $100\,000 \text{ cm}^2/\text{Vs}$ has been measured. To study electron transport across the heterojunctions, the wafer was processed into a two-level transistor mesa structure shown schematically in Fig. 1a. Evaporated AuGeNi alloy

contacts were made to the InAs, the n⁺ buffer and the cap n⁺ GaSb layers. This was followed by a rapid annealing to form ohmic contacts.

With the InAs region at ground potential, the current/voltage (*I/V*) characteristics at room temperature for the GaSb/InAs and the AlSb/InAs heterojunctions are shown in Figs. 2a and b, respectively. For the GaSb/InAs heterojunction under forward bias, the linear region gives an ideality factor $n = 1.14$. The barrier height at zero bias can be estimated from $\phi = (kT/q) \ln(AT^2/I_s)$, where A is the effective Richardson constant and I_s is the saturation current density at zero voltage. Assuming $A \sim 5 \text{ A cm}^{-2} \text{ K}^{-2}$ for GaSb, a barrier height of $\phi \sim 0.6 \text{ eV}$ is obtained. The confinement energy of the InAs quantum well is around 0.1 eV, as is the Fermi energy, giving a conduction band offset of about 0.8 eV between InAs and GaSb. This value is consistent with the established values in this material system.⁷

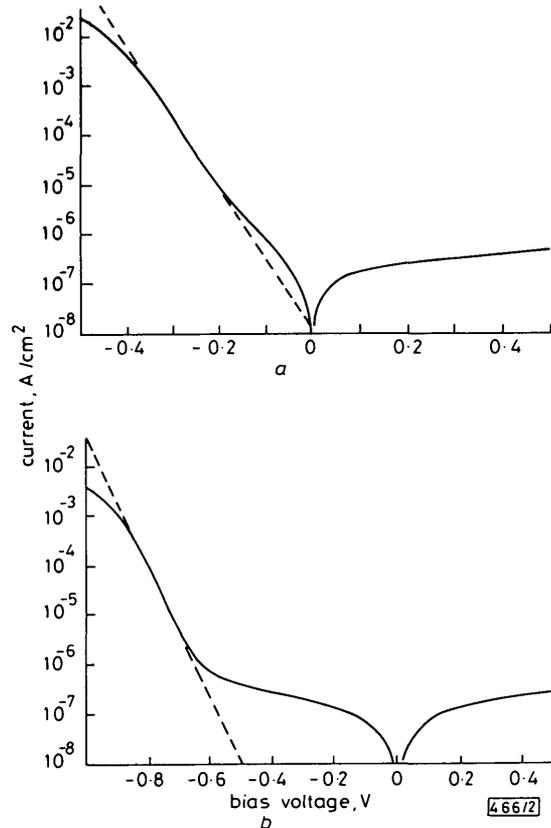


Fig. 2 Current/voltage characteristics of (a) GaSb/InAs and (b) AlSb/InAs heterojunctions measured at room temperature

For the AlSb/InAs heterojunction under forward bias, the linear region of the diode characteristics gives an ideality factor of about 1.3. The excess current of around 10^{-7} A is

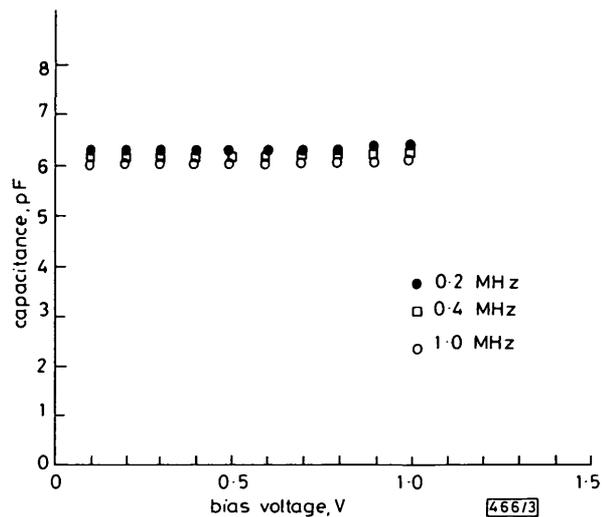


Fig. 3 Capacitance/voltage characteristic of AlSb/InAs heterojunction measured at 77 K at different frequencies

probably related to dislocations. We hope to reduce this excess current by the incorporation of As to form AlSbAs lattice-matched to the GaSb substrate. The AlSb/InAs heterojunction has a staggered band line-up with a large energy band discontinuity of 1.3 eV occurring in the conduction band. Our device structure employs a thin 1000 Å unintentionally doped AlSb barrier layer, followed by heavily Te-doped n^+ thin AlSb and GaSb layers for ohmic contact. Consequently the electrical barrier thickness is expected to be a constant equal to the thickness of the intrinsic AlSb region, characteristic of a Mott barrier.⁸ This can be characterised by a capacitance/voltage (C/V) measurement showing essentially constant capacitance. Results of our C/V measurements for modest forward bias are illustrated in Fig. 3. The lack of frequency dependence in the C/V profile suggests that deep levels in the AlSb layer can be ignored in the present device structure.

In summary, we have described the successful growth AlSb/InAs/GaSb double heterostructures with abrupt interfaces by MBE. Room-temperature current/voltage measurement shows good electrical quality of the GaSb/InAs and AlSb/InAs heterojunctions. Low-temperature capacitance/voltage measurement establishes that the intrinsic AlSb barrier is a Mott barrier with few deep levels. Our test structure suggests that double heterojunction hot-electron devices with base transit regions as thin as 100 Å operated at room temperature can be realised in the AlSb/InAs/GaSb material system.

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1st June 1987

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