Control of a natural permeable $CoSi_2$ base transistor

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We report results on the fabrication of a natural permeable base transistor in a $Si/CoSi_2/Si$ heterostructure using molecular beam epitaxy (MBE). No photolithography is required, the transistor action being controlled by MBE growth conditions through the density and size of natural openings in the silicide base. The electrical characteristics of devices processed from such heterostructures are intimately related to the presence of these openings. Common base current gains in the range 0.01–0.95 have been observed and correlated with the size and density of the openings.

In recent years considerable interest has centered on the fabrication of a permeable base transistor (PBT) in silicide.[1,2] This is in part due to potential device applications involving operation at high frequencies. Traditionally PBT's have been fabricated by lithographically defining a grid of metal electrodes with submicron spacing which control current flow through the transistor. Silicon PBT's have recently been reported with a short-circuit unity-current-gain frequency of over 20 GHz[2] with gallium arsenide achieving even better performance.

Previously we reported transistor action in a silicon-metal-silicon structure.[3] The metal used was $CoSi_2$ and the entire single crystal $Si/CoSi_2/Si$ heterostructure was grown without breaking vacuum using molecular beam epitaxy (MBE). $CoSi_2$ was chosen because of its low resistivity at room temperature, its epitaxial growth on Si, and because epitaxial Si overgrowth is also possible.[4] In this letter we report results of detailed investigations on this structure which have revealed a mode of operation resembling a PBT rather than a metal base transistor. Electron transport occurs entirely in silicon through naturally formed openings in the metal base. In particular, there is no evidence for ballistic transport through the structure as originally reported by Rosencher *et al.*[5] The fabrication of the novel[6] PBT described in this letter avoids the problems inherent to submicron lithography or silicon overgrowth on a substrate which has been exposed to atmosphere. In addition we have been able to control the average size, distribution, and density of openings in the single crystal metal (transistor base) layer and demonstrate the relationship between transistor action, growth conditions, and microstructure.

The samples described in this letter were grown in an ultrahigh vacuum (UHV) chamber which had a base pressure of less than 1×10^{-10} Torr. Prior to crystal growth n-type (impurity concentration $n = 0.3\text{–}2\times10^{17}$ cm^{-3}) silicon substrates of (111) orientation were cleaned using the Shiraki method.[7] Silicide growth was achieved by depositing an approximately 15–40-Å thick film of Co, in some cases a thin Si layer was also evaporated, then the substrate temperature was raised to 550 °C or above for around 3 min by resistive heating. After formation of a 55–145-Å $CoSi_2$ film in this fashion, 1500 Å silicon was grown epitaxially over the metal film at a rate of 1–3 Å/s at ~610–640 °C. Occasionally, a thin template (10–50 Å) of Si was first deposited at room temperature on the silicide and annealed to ~600 °C for 1 min before subsequent Si evaporation. *In situ* low-energy electron diffraction (LEED) and Auger were used to monitor the growth. The overgrown silicon was doped n type using flux from a Sb effusion source. The impurity concentration was determined by the growth temperature[8] and was typically of order $n = 10^{16}$ cm^{-3}. In some experiments an undoped Si layer ~1000 Å thick was first grown on the silicide. No impurities were found on the surface by Auger analysis after such a deposition, and sharp 7×7 LEED patterns were observed. A portion of the heterostructure thus formed was reserved for later structural studies. Ohmic contact to the overgrown silicon was made by co-depositing Si and Sb at room temperature to give a heavily doped 500-Å-thick n^+ amorphous cap. The cap layer was then crystallized by annealing at 600 °C. Metallization to the n^+-Si layer was achieved by depositing 200 Å of Co with the substrate at room temperature.

The grown epilayers were then removed from the UHV chamber and fabricated into a two level mesa structure using a dry etch technique to reveal the three active layers. Electrical contacts were made to the Co metallized surface layer (emitter, ~200 μm diameter), the thin-film $CoSi_2$ layer (base, ~300 μm diameter), and to the back of the Si substrate (collector). The large area collector contact was achieved by Sb evaporation followed by laser alloying.

Samples were characterized by transmission electron microscopy (TEM) and Rutherford backscattering and channeling (RBS). Samples for TEM were chemically thinned for plan view or ion thinned for cross section. For plan view observation, Si overlayers were thinned to improve the visibility of $CoSi_2$ layers. Silicide layers grown above 600 °C are essentially single crystals of the B orientation.[9] Fractions of A-oriented $CoSi_2$ are also found and can be affected by Si deposition in conjunction with Co deposition. A characteristic of all $CoSi_2$ layers is the presence of small openings ("pinholes") and a fairly regular network of misfit dislocations [e.g., for B-type layers $b = (a/6)\langle112\rangle$ spacing $\simeq 300$ Å] at the substrate $Si/CoSi_2$ interface.[9] These features are found both in films grown with and without Si overlayers. In the $Si/CoSi_2/Si$ heterostructure pinholes are filled with columns of Si, revealed in images of cross-section samples.

Overgrown Si layers contain a lower density of misfit dislocations at the $CoSi_2/Si$ interface but several propagate through the layer and there are a number of stacking fault tetrahedra. Nevertheless, the overall quality of the Si overlayers is good, as measured by ion channeling, with a χ_{min} of less than 4%.

Figure 1 is a series of bright-field plan view TEM images

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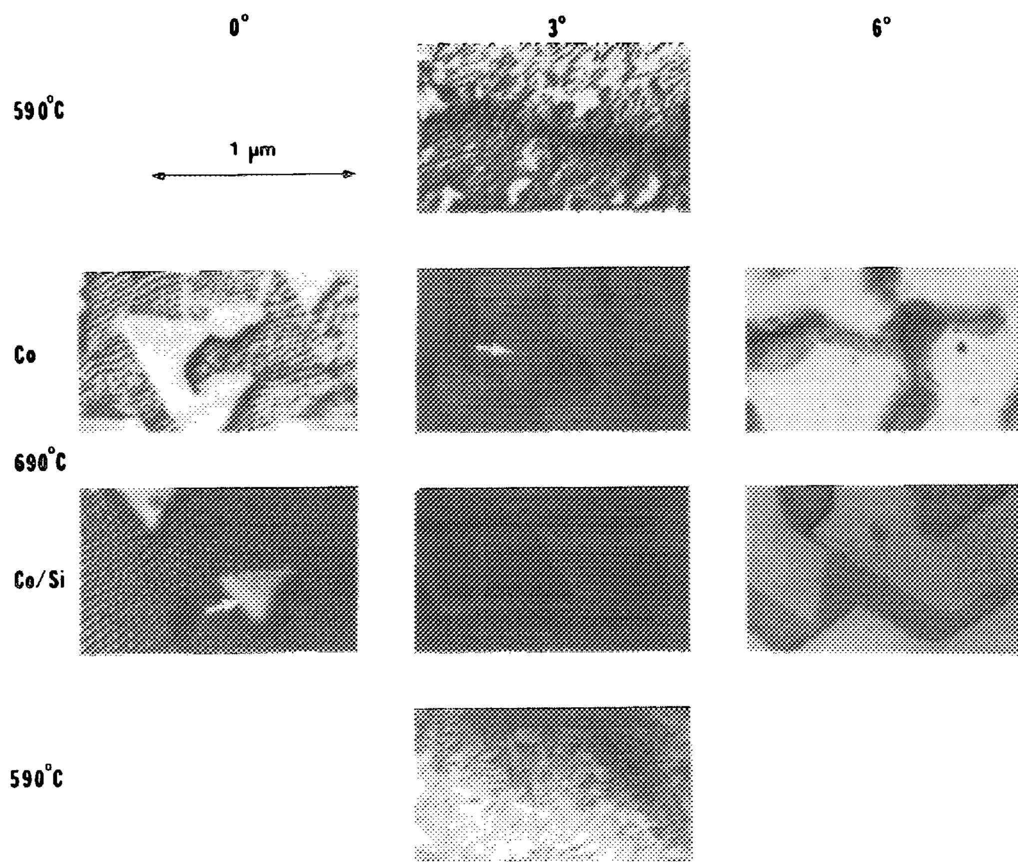

FIG. 1. Two-beam bright-field images of various thin $CoSi_2$ films on Si in plan view. Pinholes appear as areas from which Moire fringes are absent. The figure shows the dependence of pinhole parameters on growth conditions. Co and Co/Si refer to the presence or absence of a Si layer deposited at room temperature along with Co; 590 and 690 °C refer to the silicide annealing temperature; 0°, 3°, and 6° refer to wafer miscut from (111).

of thin $CoSi_2$ layers ($\sim$90 Å thick). The images were taken with a (220) reflection common to type *A*- and *B*-oriented $CoSi_2$ and Si. Pinholes are clearly visible as regions from which Moire fringes are absent, such as the arrowed areas. Moire fringes arise from the misfit dislocation network primarily between the substrate Si and $CoSi_2$ layer. Some pinholes are triangularly shaped with sides in the ⟨110⟩ direction. This direction arises from the inclined ⟨111⟩ facets which occur at the edges of the pinholes.

More direct observation of pinholes in the $CoSi_2$ layer comes from mapping both the *A* and *B* regions of the silicide using Bragg reflections forbidden for silicon [e.g., (200)]. This painstaking method shows that the simple absence of Moire fringes in an image taken with common reflections is, in fact, a reliable technique with which to detect pinholes. It can be seen from Fig. 1 that pinhole parameters such as mean diameter X, standard deviation Y, and fractional areal coverage Z, are strong functions of silicide growth conditions. Growth conditions which have been shown to have a significant effect include the ratio of Si/Co in the initial deposition, the temperature of the $CoSi_2$ growth, the angle of miscut from the (111) orientation of the substrate, and the silicide thickness. We note that this technique can give us access to dimensions that are currently unobtainable using lithographic methods. To grow the most uniform $CoSi_2$ layers it is necessary to use ratios of Si/Co$\sim$1, temperatures of less than 600 °C, substrates cut to exactly (111) orientation, and $CoSi_2$ thicknesses of $\sim$60–90 Å. Any departure from these conditions results in an increase in the size and density of the openings. Room-temperature deposition of a thin Si layer following the Co deposition helps to reduce the size and density of openings as well as nearly eliminate the type *A* $CoSi_2$ grains. With miscut Si (111) substrates, an optimized Si/Co ratio also helps in achieving a more peaked distribution of pinhole sizes.

The crystalline structure of overgrown Si is controlled by the use of thin "templates" deposited at room temperature on the $CoSi_2$ film. Under certain circumstances, the orientation of the Si layer can be made either pure *A* or *B*. We have found that type *A* Si can be grown on perforated $CoSi_2$ layers which contain a substantial fraction of type *A* $CoSi_2$ grains. Type *B* Si grows with use of a Si template on very uniform $CoSi_2$ of pure *B* orientation. In general, the Si orientation depends on the orientation of the silicide, the pinhole dimension, the Si template, and the wafer miscut. RBS spectra demonstrate these results and the high quality of overgrown silicon in all cases (see Fig. 2).

Devices fabricated from these heterostructures were first described in a previous publication.[3] We have found a strong correlation between the distribution of pinholes seen by TEM and device characteristics, in particular the common base current gain α. This strong evidence leads us to conclude that electron transport through the base occurs exclusively through pinholes. This is in disagreement with the conclusions of Rosencher *et al.*[5] who have considered electrical transport through similar structures. We believe the transistor action is of a permeable base nature, i.e., charge transport occurs through pinholes in the $CoSi_2$ metal base. The largest α observed for almost pinhole-free silicide is $\sim$0.01, setting an upper limit on the magnitude of ballistic transport through the metal base. An explanation for the lack of any ballistic transport may be the absence of suitable electronic states extending from the silicon conduction-band minimum and through the $CoSi_2$ metal.

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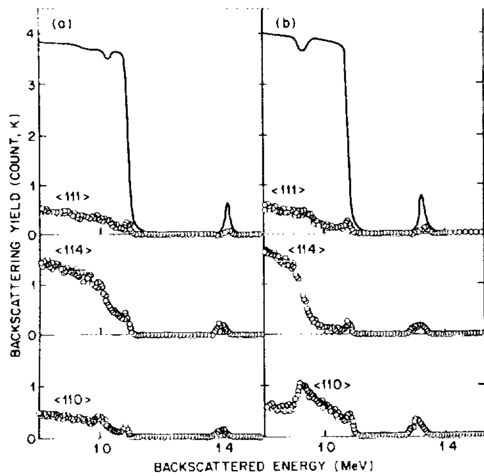

FIG. 2. Channeling and random RBS spectra from $Si/CoSi_2/Si(111)$ structures. Surface inclined channeling characteristics can provide information on the orientation of the layers (see Ref. 7); (a) a type A Si overlayer grown on mixed $A + B$ $CoSi_2$ and (b) an essentially ABB heterostructure.

In Fig. 3 we show common base and common emitter current-voltage characteristics for two typical samples, one with $\alpha \cong 0.12$ and another with $\alpha \cong 0.6$. We have observed a strong correlation between α and the size and density of pinholes in all the devices we have tested. Careful experiments in which only X, Y, and Z were varied gave, for example, $\alpha \cong 0.12$, $X = 2000$ Å, $Y = 250$ Å, $Z = 0.18$ and $\alpha \cong 0.08$, $X = 1300$ Å, $Y = 500$ Å, $Z = 0.14$. Measured α's have ranged from greater than 0.95 for highly perforated films to less than 0.01 for almost pinhole-free $CoSi_2$ films. We have been unable to grow completely pinhole-free $CoSi_2$ films, even though our growth conditions were similar to Ref. 5.

It is possible to model the current-voltage characteristics of the device by considering the effect that a small pinhole has on the $Si/CoSi_2$ Schottky barrier. We assume that the $Si/CoSi_2$ interface pins the barrier at $\phi_B = 0.64$ eV, impeding charge transport from emitter to collector. A small opening in the $CoSi_2$ film connecting emitter and collector by a column of Si also presents a potential barrier to charge transport. The barrier energy is pinned to ϕ_B at the edge of the pinhole and, assuming a circular opening, decreases approximately parabolically to a minimum $\phi_B - \Delta_0$ at the center of the hole. Assuming charge transport to be governed by standard thermionic emission theory, then an expression for α is

$$\alpha = \xi / (\gamma + \xi) , \quad (1)$$

where

$$\xi = \frac{k_B T}{e\Delta_0} \left[\exp\left(\frac{e\Delta_0}{k_B T} \right) - 1 \right] ,$$

$\gamma = (1 - Z)/Z$, k_B is the Boltzmann constant, T the temperature, and e the electronic charge. Equation 1 has been used to model our current-voltage characteristics, and good qualitative agreement has been obtained with the experimental results. The model also predicts the observed correlation between α and pinhole distribution. These calculations are only in qualitative agreement with the measurements, α's consistently being less than those expected from TEM. This is due to uncertainties in doping level near pinholes and crystalline imperfections.

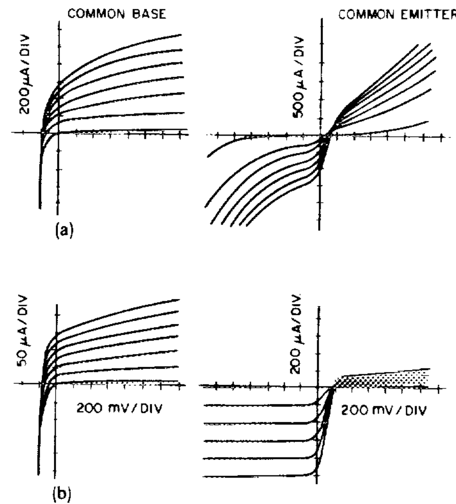

FIG. 3. Device current-voltage characteristics in the common base and common emitter configuration for a sample with $\alpha \cong 0.6$ shown in (a) and $\alpha \cong 0.12$ shown in (b). Curves were taken in steps of 200 μA beginning with $I_{cc} = 0$.

The natural permeable base transistors we have fabricated from our $Si/CoSi_2/Si$ heterostructures have been successfully operated as amplifiers exhibiting significant ac voltage gain at frequencies greater than 10 MHz, performance in this case being limited by the test circuit used. However, we note that the ultimate speed of this promising device will be attained when crystal growth conditons have been optimized to give a high α and a sharply peaked distribution of pinhole sizes.[10]

In conclusion, we have reported the fabrication of a novel natural permeable base transistor grown in a $Si/CoSi_2/Si$ heterostructure using MBE. Transistor action has been demonstrated in this structure, and electrical performance has been correlated with growth conditions. We have shown that charge transport in these heterostructures is associated with pinholes and have found no evidence for direct[5] transport through the metal base.

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