Chip Scan: 3D X-ray imaging of CMOS integrated circuits

A.F.J. Levi
University of Southern California
Department of Electrical and Computer Engineering
alevi@usc.edu
https://alevi.usc.edu/

MQRW Aerospace Corporation, 240 S. Douglas St., El Segundo, CA 90245
8:15 AM, Tuesday, 11 February 2025

Motivation

Legacy iPhone 14 integrates many small chips (most of area < 54 mm^2)

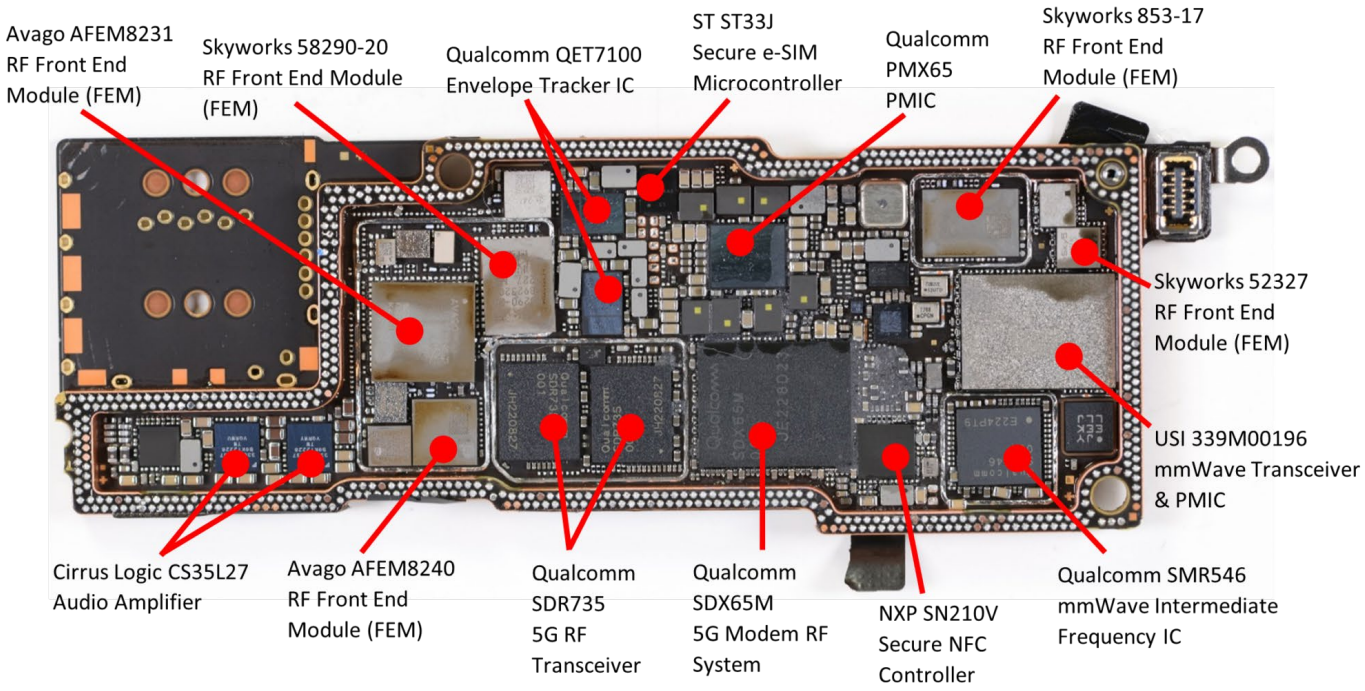
What do these chips *do*, and what can the system *do*? Are these and future chips *reliable* and *trustworthy*? Are any of these chips counterfeit, do they contain defects, or have they been modified for other purposes?

Apple shipped a total of 92 million iPhone 14 models globally in 2023 that include an A16 Bionic processor with 16B transistors in 113 mm^2 area, a 3.5GHz clock, and manufactured in the TSMC N4 process

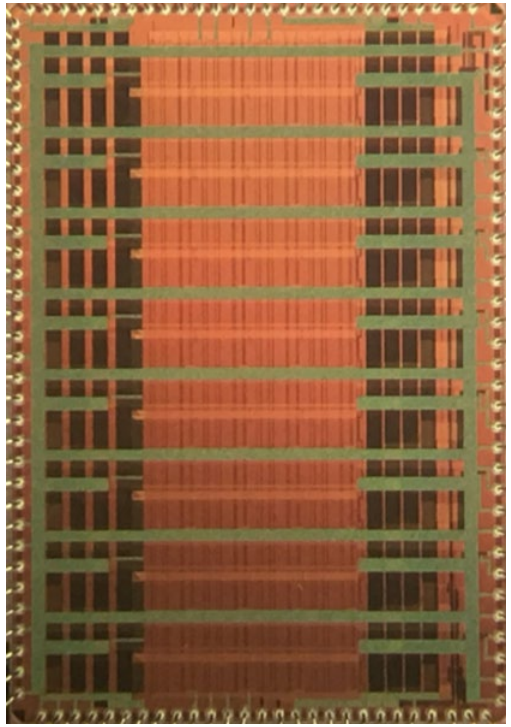
Example of RFFEM component:
[Skyworks SKY-58260-11 RFFEM]
PA blocks, input and output matching, a MIPI standard digital control block, single-ended duplexers, antenna and band select switches, and LNA in a single 79-pad surface mount 6.4 mm x 5.0 mm x 0.85 mm package.

- 5G commercial applications
- Multi-band 4G/3G handsets- WCDMA Bands 5, 8 and CDMA BC0, BC10
- LTE Bands 8, 12, 13, 14, 20, 26, 28, 29, 71- Up to 20 MHz bandwidth

Example of *legacy* iPhone 14 Pro components:

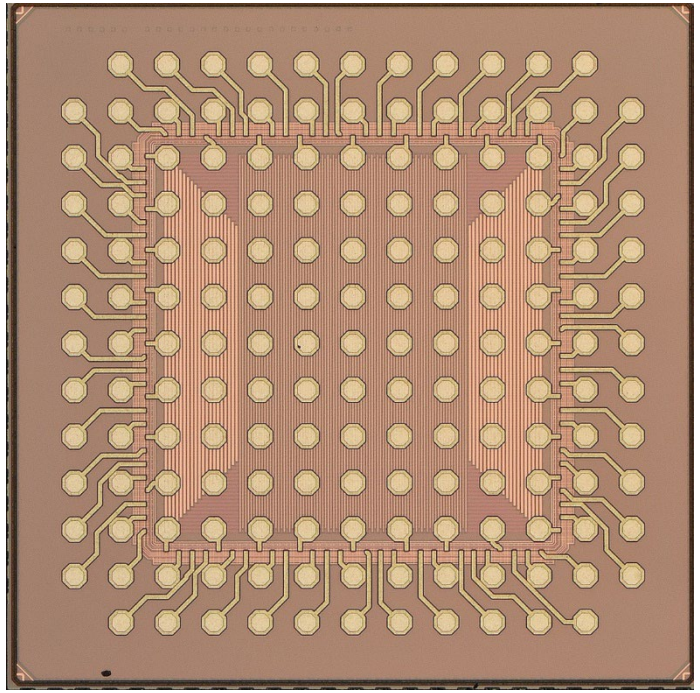


And, in the future, can we figure out what custom circuits do?

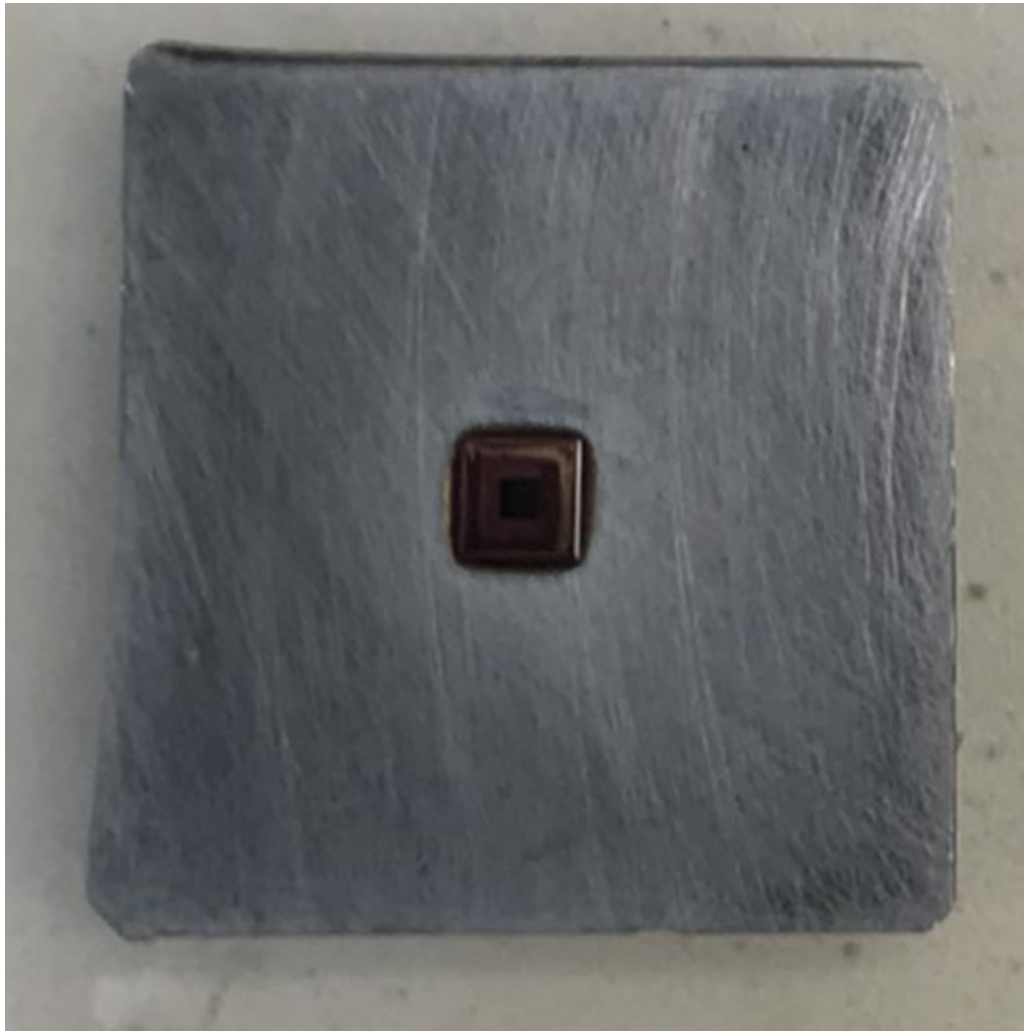


A basic question: Can you trust the electronic hardware you use?

Conventional chip-level inspection: a *destructive* delayering process



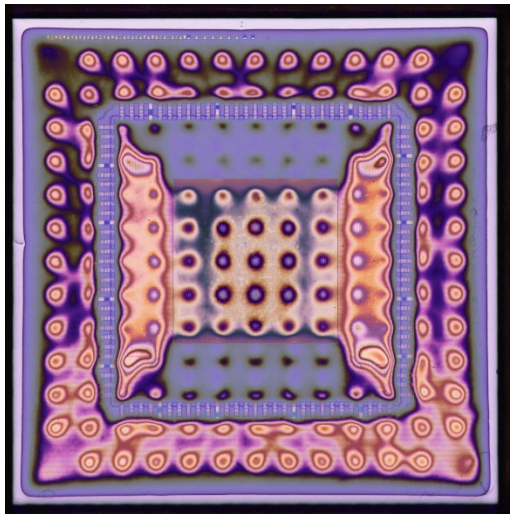
- Optical photograph of CMOS encryption engine test die
- 2.5 x 2.5 mm^2 area
- 13 x 13 – 4 = 165 solder bump pads
- 170 µm pitch, 89.04 µm diameter, 80.96 µm space



- Chip mounted on a mechanical polishing block as an initial step in the destructive delayering process

Conventional chip-level inspection: a *destructive* delayering process

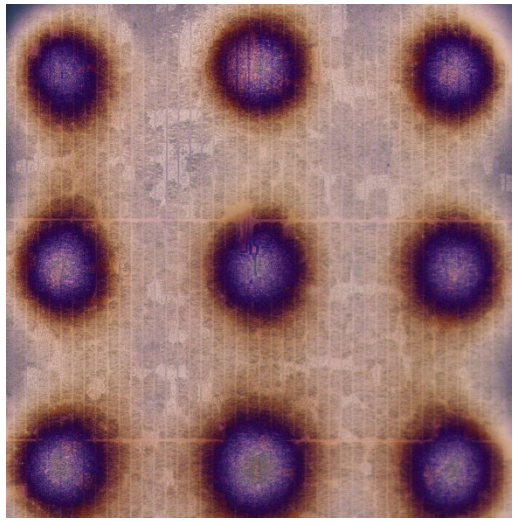
- *Destructive* mechanical (or ion-beam) polishing to delayer chip
  - Even though this can be *automated*, the process is slow, with scanning electron microscope (SEM) imaging at each layer
  - Because this is a *destructive* method, reinspection of a destroyed layer is not possible
  - Mechanical processes can introduce damage at the nm scale
  - Non-planar structures difficult to reconstruct



Optical microscope image

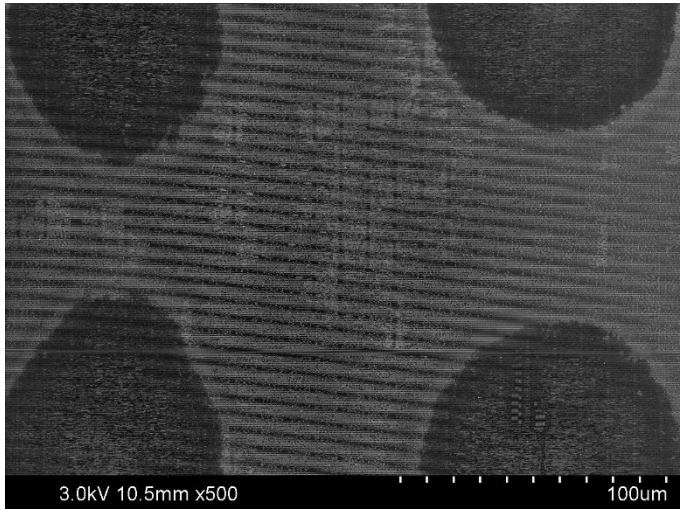
2.5 x 2.5 mm^2 chip area

0.9 x 0.9 mm^2 circuit area



Optical microscope image

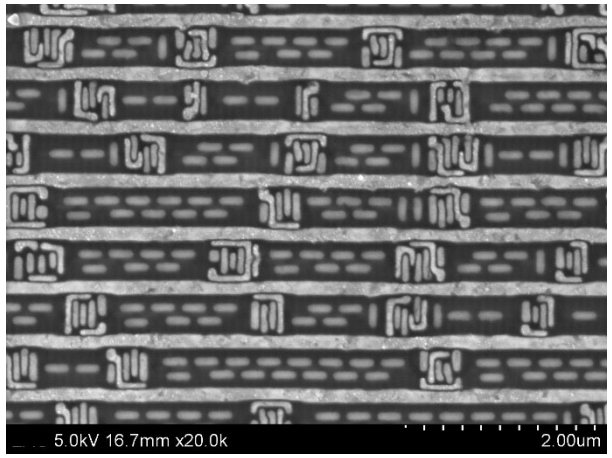
Solder bumps with 170 mm pitch, 89.04 mm diameter



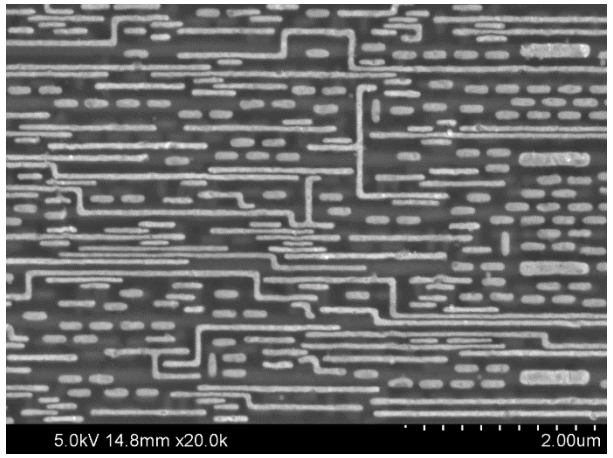
SEM image

Solder bumps with 170 mm pitch, 89.04 mm diameter, 80.96 mm space

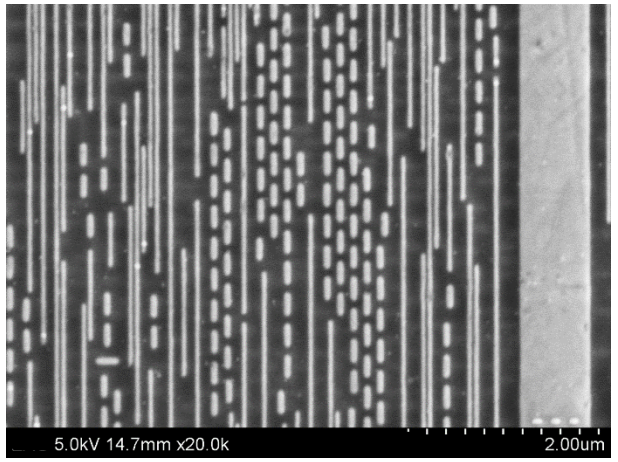
M1



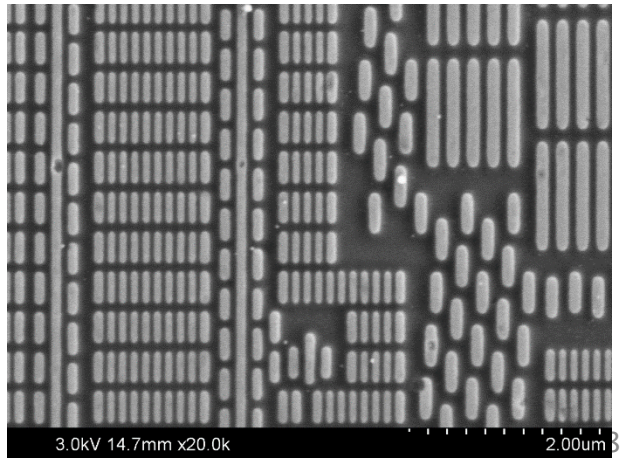
M2



M3



M7



Non-destructive chip inspection using coherent X-ray 3D imaging

Chip Scan: 3D X-ray imaging of CMOS circuits at nm-scale

- The objective is to rapidly find out "*what's inside*" any integrated circuit
- Non-destructive lensless coherent X-ray diffraction computational 3D-imaging of advanced-technology CMOS integrated circuits

Key contributors to the team effort: Tomas Aidukas, Mirko Holler, Manuel Guizar-Sicairos, Michal Odstrcil, Elisabeth Müller, Ana Diaz, Gabriel Aeppli, and A. F. J. Levi

Publications: M. Holler et al., *Nature Electronics* **2**, 464 (2019)

A.F.J. Levi and G. Aeppli, spectrum.ieee.org/chip-x-ray (2022)

I. Kang et al., *Optica* **10**, 1000 (2023)

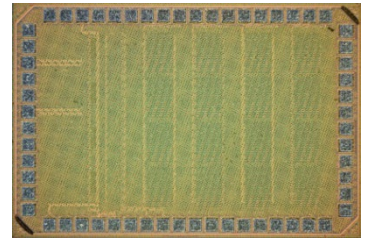
T. Aidukas et al., *Nature* **632**, 81 (2024)

Recent progress: Compared to 2019: Optimization of hardware *and* algorithms gives10x increase in depth of field to 5µm using filtered backpropagation tomography, 4x improvement in resolution to 4 nm using burst ptychography to remove experimental instabilities, 16x speedup using ML

Future work: 100x brilliance *after* synchrotron upgrade in 4Q25, 100x flux with new X-ray optics in 4Q25, 3D reconstruction of integrated circuits with potential sub-nm resolution, speedup with new hardware and algorithms, speedup with ML and AI, integration with XRF for trace detection and multimodal imaging

USC

USC-designed digitizing matrix-multiplier chip for Machine Learning manufactured by Global Foundries in 2017 in 14 nm FinFET CMOS technology



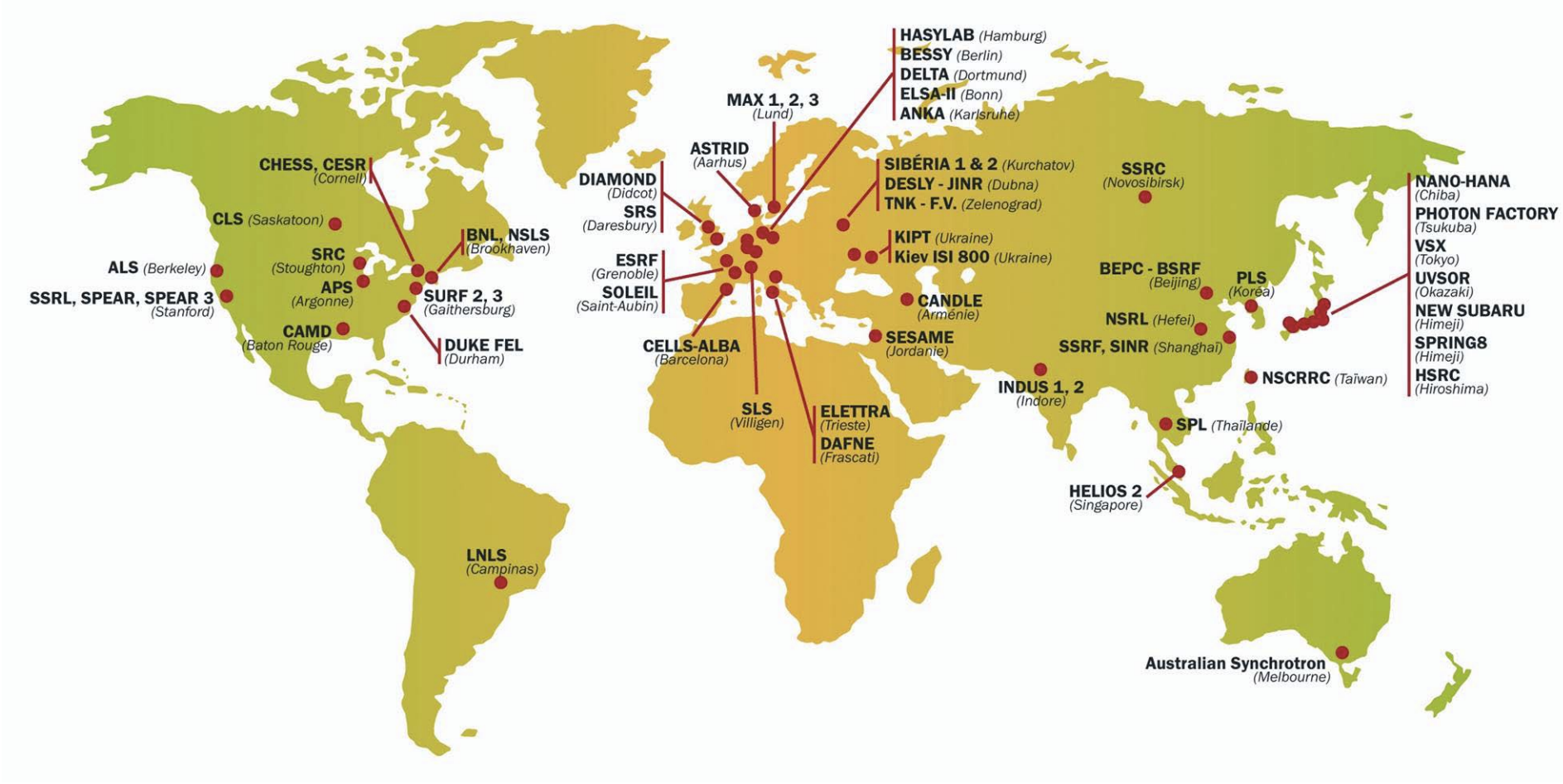
GlobalFoundries Inc.

Swiss Light Source (SLS) at PSI, ETH-Zurich

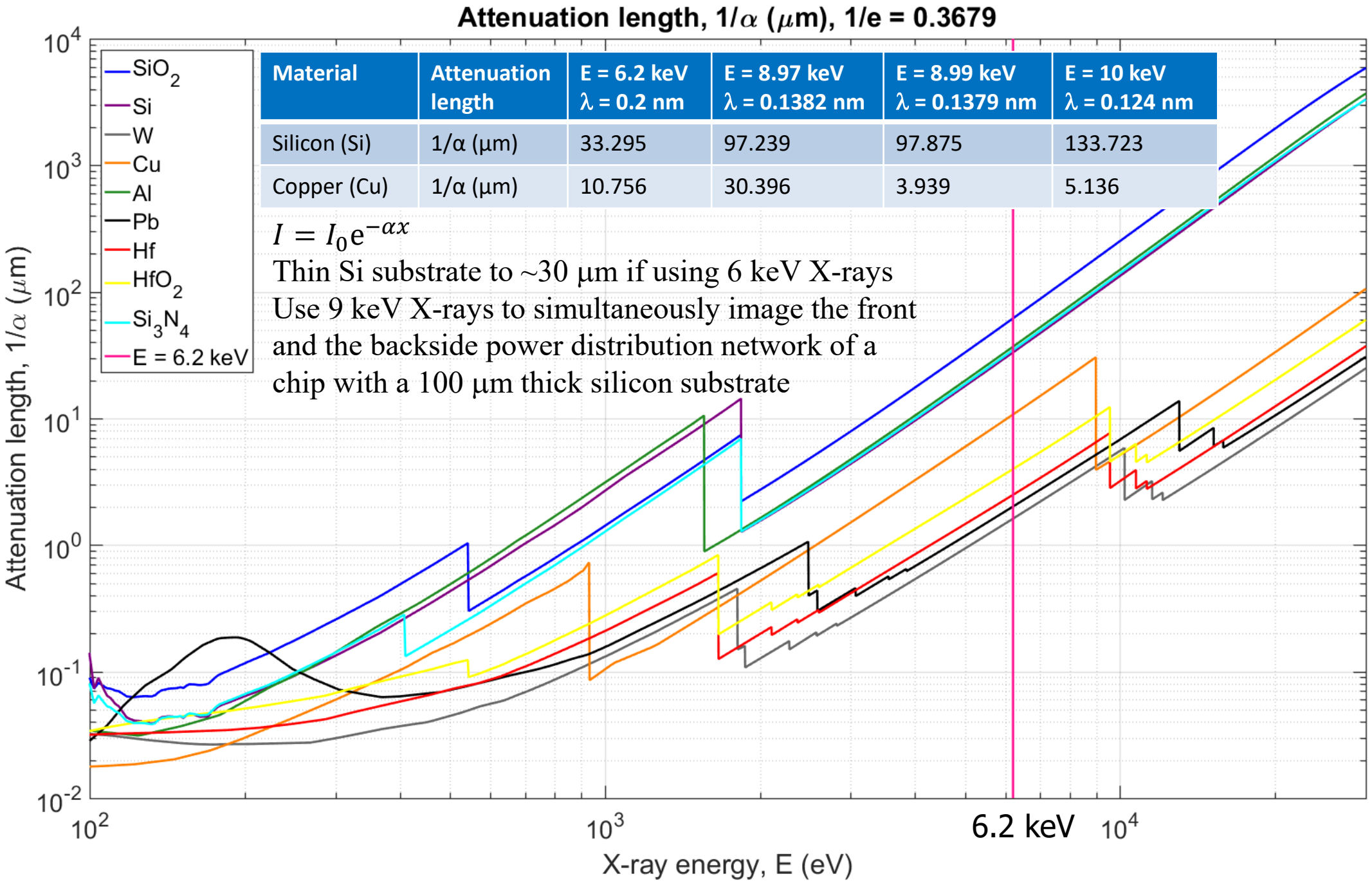
CSAXS 6 keV photons, 0.2 nm wavelength
2024 coherent photon flux at sample 7×10^8 s^{-1}

Synchrotron X-ray sources

- Synchrotron coherent X-ray sources
- An established and mature technology
- Globally, there are about 50 storage-ring based systems in use
- More than 60,000 users



X-ray properties of materials

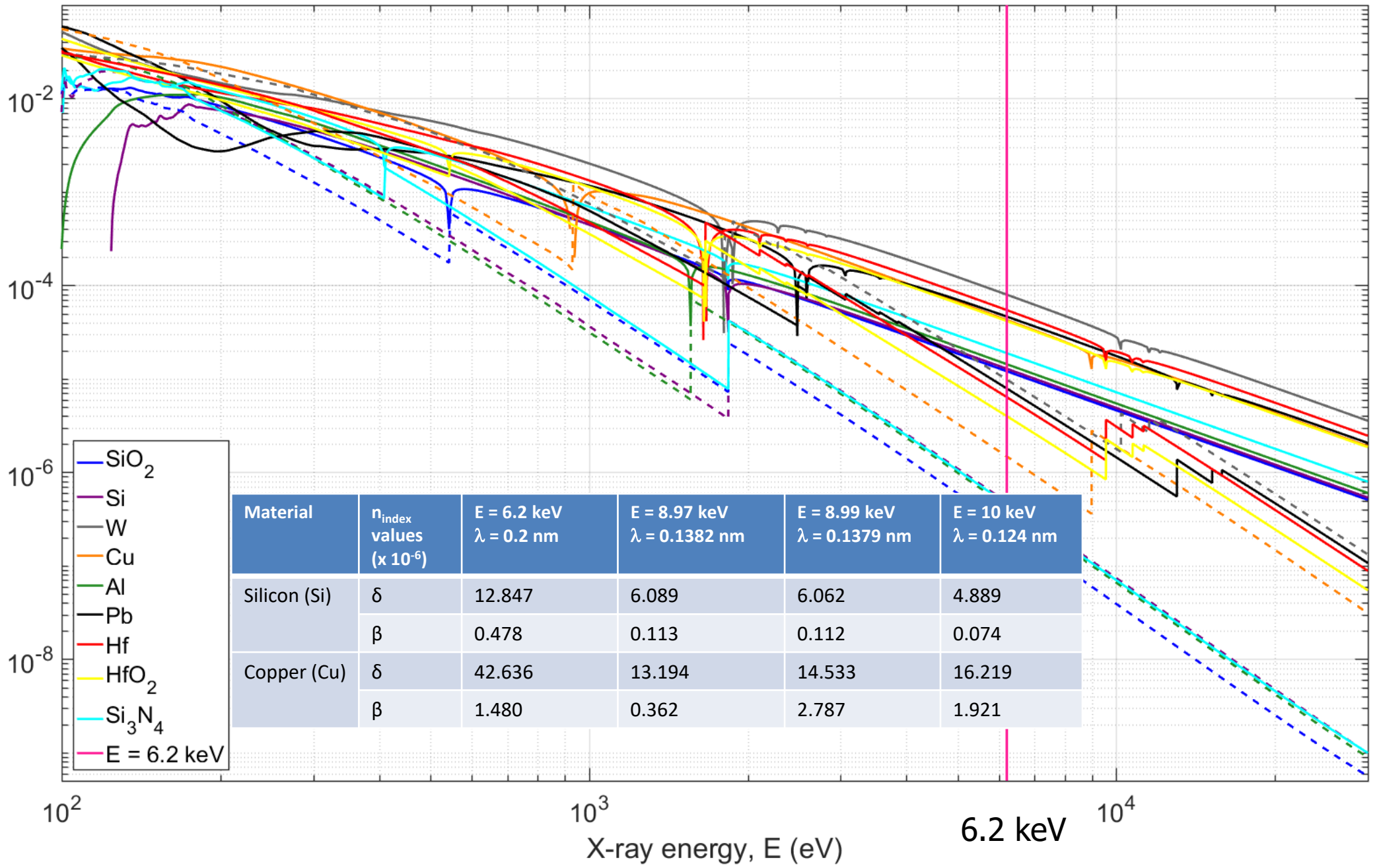


Material	Attenuation length	E = 6.2 keV λ = 0.2 nm	E = 8.97 keV λ = 0.1382 nm	E = 8.99 keV λ = 0.1379 nm	E = 10 keV λ = 0.124 nm
Silicon (Si)	1/α (μm)	33.295	97.239	97.875	133.723
Copper (Cu)	1/α (μm)	10.756	30.396	3.939	5.136

$I = I_0 e^{-\alpha x}$

Thin Si substrate to ~30 μm if using 6 keV X-rays

Use 9 keV X-rays to simultaneously image the front and the backside power distribution network of a chip with a 100 μm thick silicon substrate

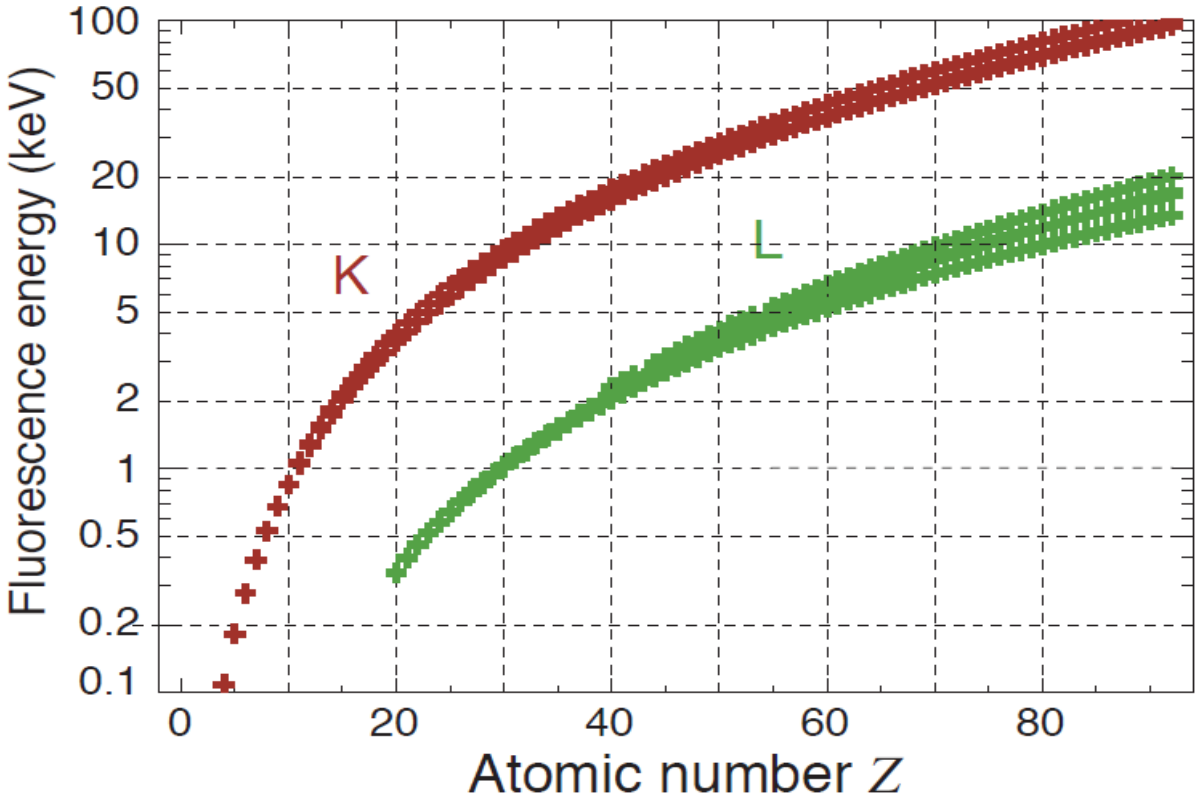


Material	n_{index} values ($\times 10^{-6}$)	E = 6.2 keV λ = 0.2 nm	E = 8.97 keV λ = 0.1382 nm	E = 8.99 keV λ = 0.1379 nm	E = 10 keV λ = 0.124 nm
Silicon (Si)	δ	12.847	6.089	6.062	4.889
	β	0.478	0.113	0.112	0.074
Copper (Cu)	δ	42.636	13.194	14.533	16.219
	β	1.480	0.362	2.787	1.921

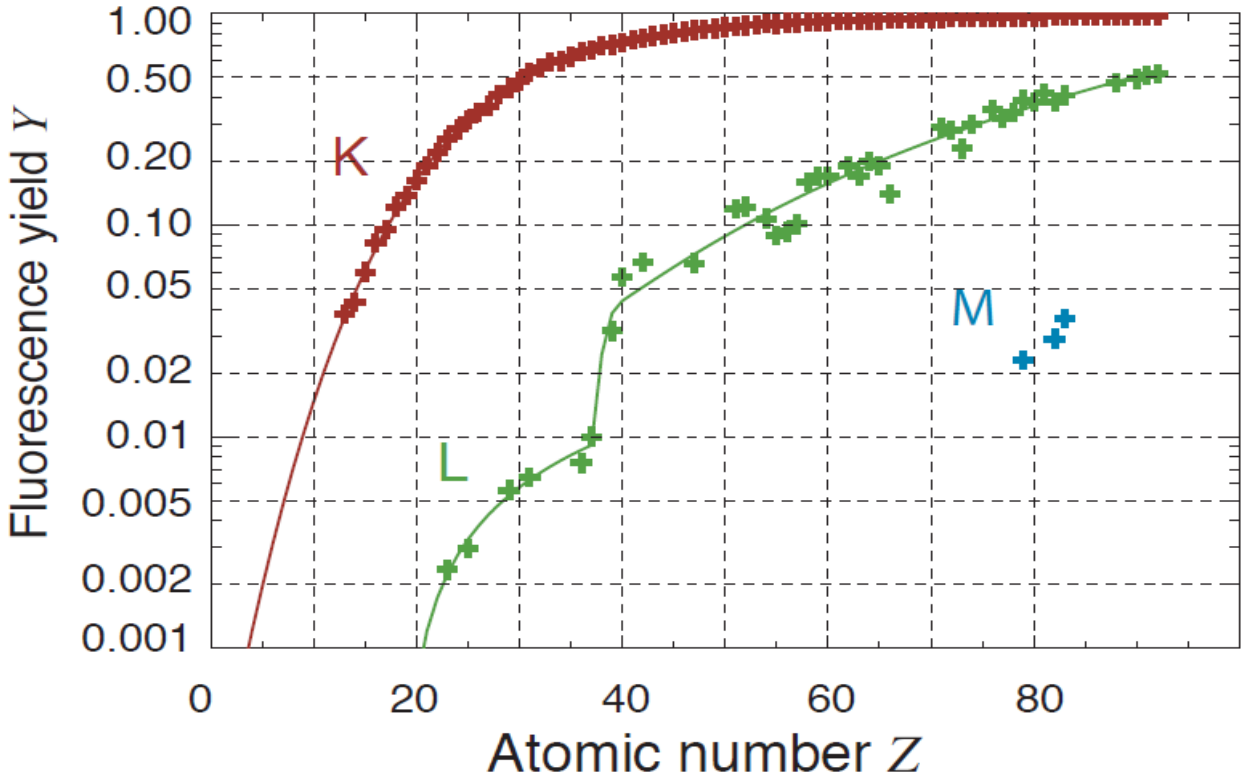
X-ray fluorescence to detect *trace* quantities of elements

Al(13), P(15), Co(27), Cu(29), As(33), Ru(44), Hf(72), Ta(73), W(74)

Fluorescence energy with atomic number

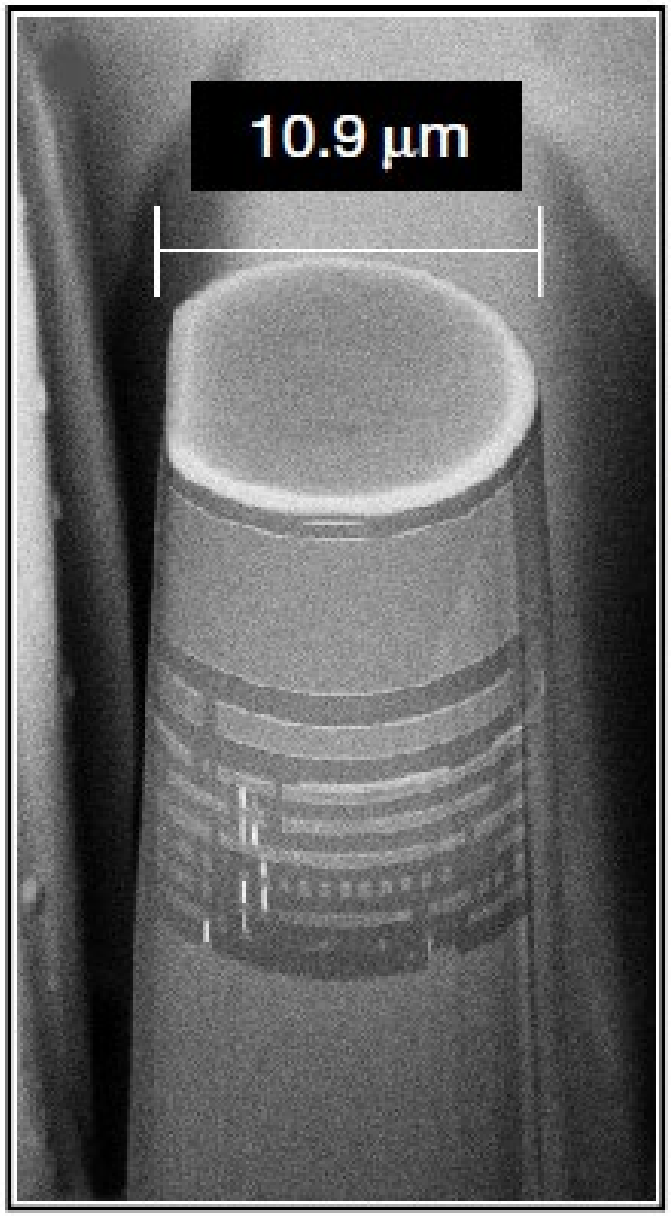


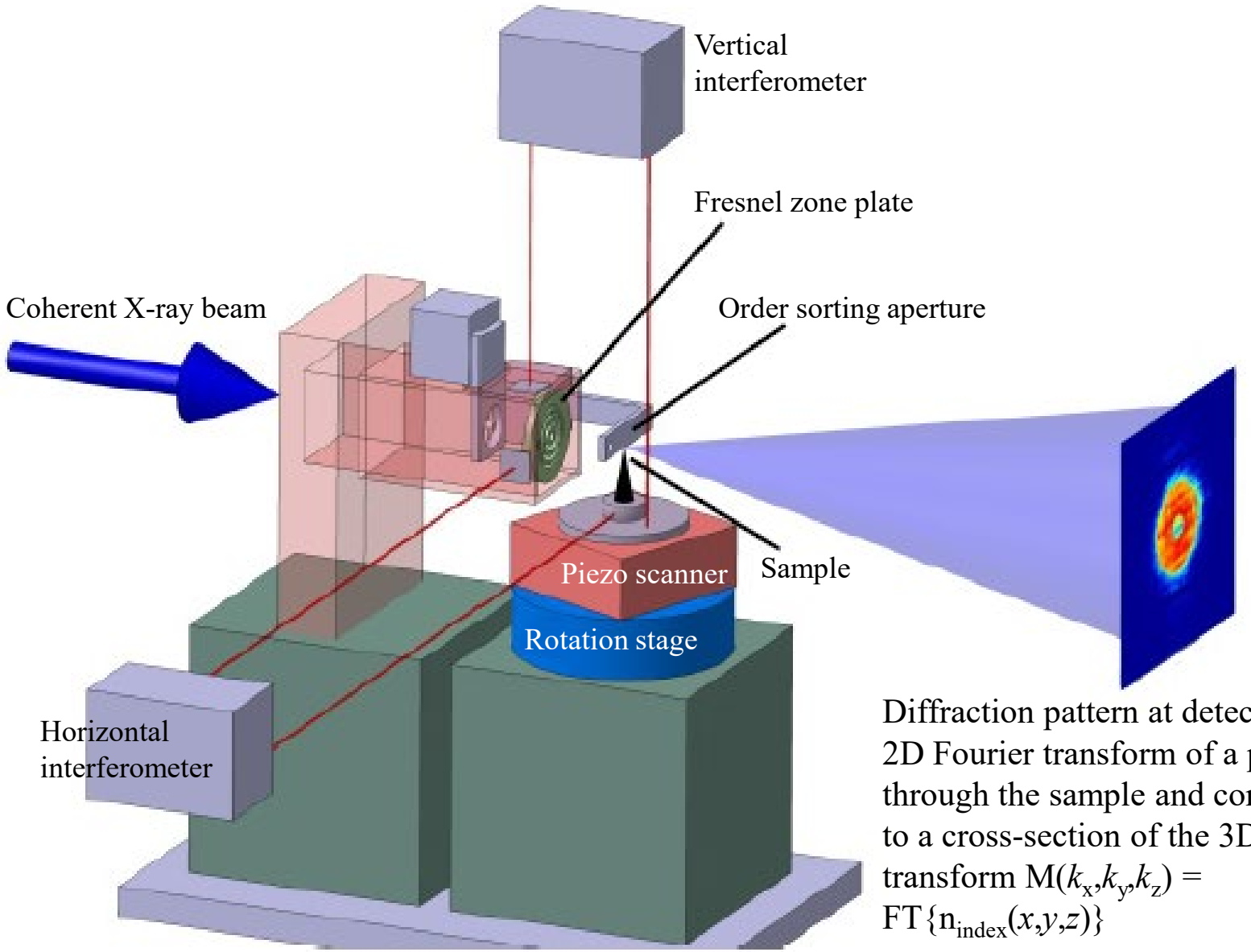
Fluorescence yield with atomic number



X-ray ptychography and 3D tomographic reconstruction

X-ray ptychography and 3D tomographic reconstruction of a small sample

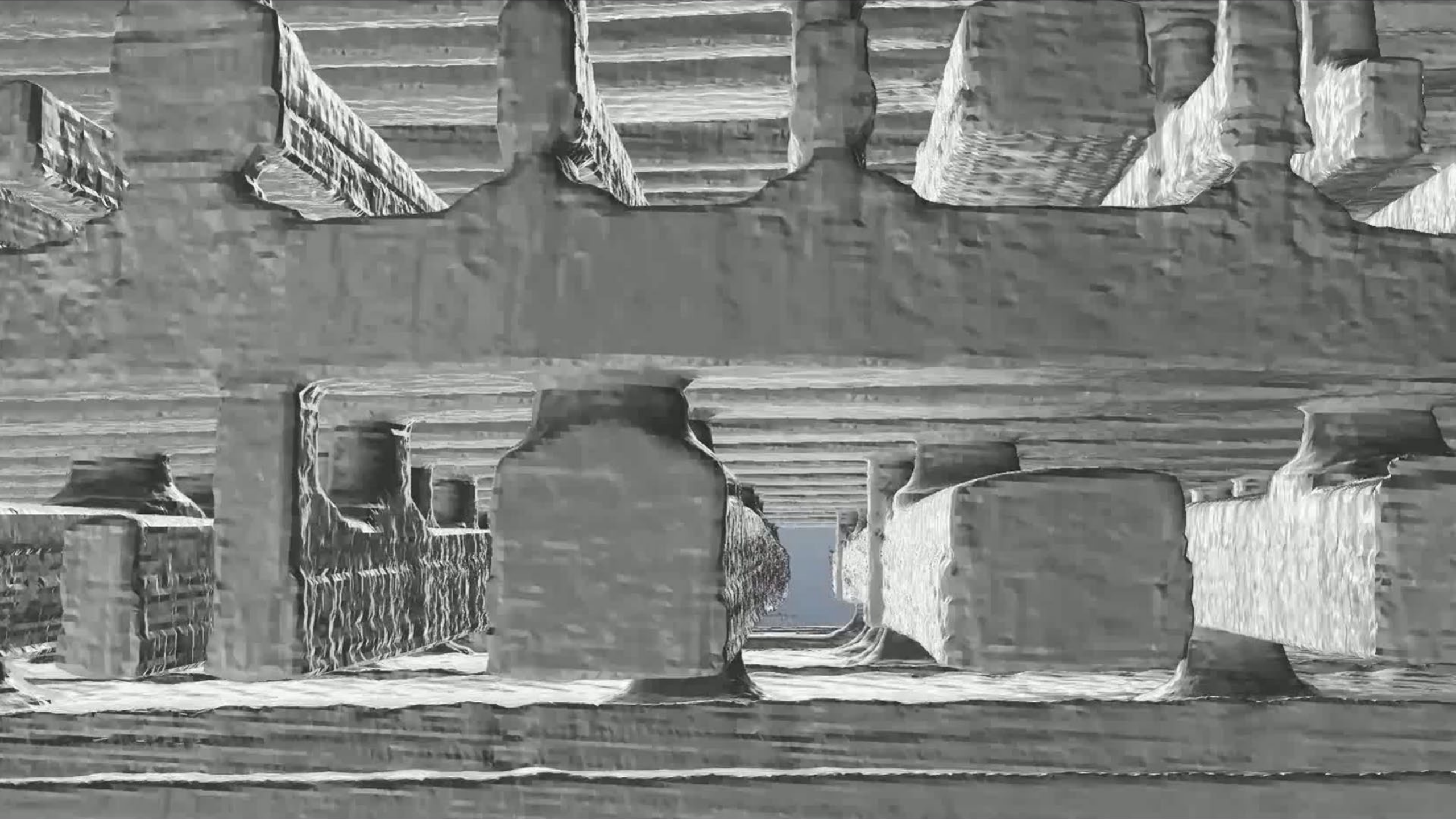


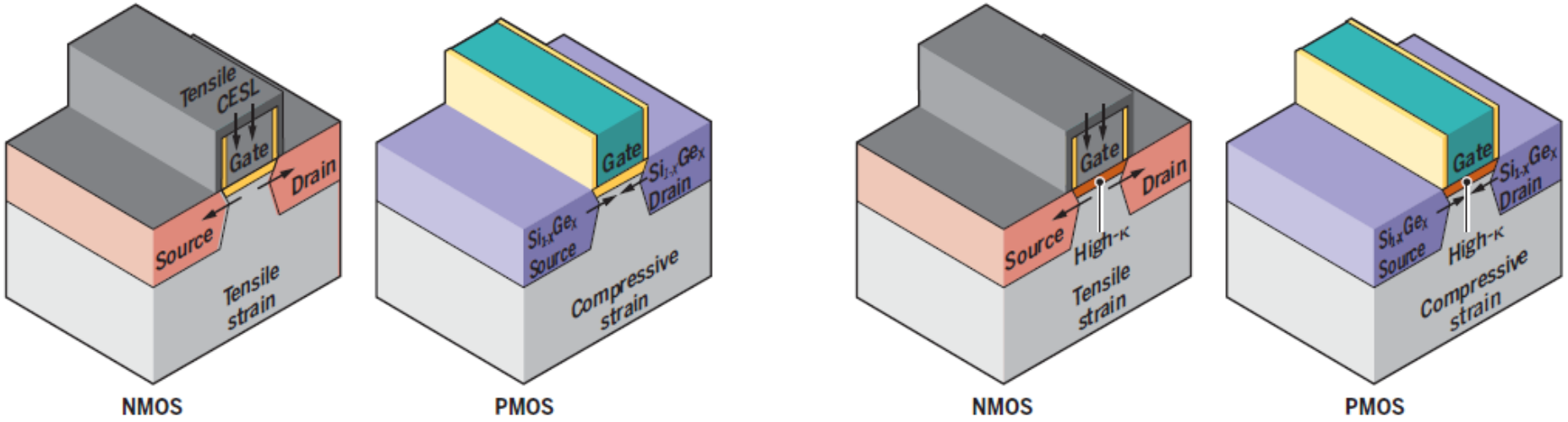


Diffraction pattern at detector is the 2D Fourier transform of a projection through the sample and corresponds to a cross-section of the 3D Fourier transform $M(k_x,k_y,k_z) = FT\{n_{index}(x,y,z)\}$

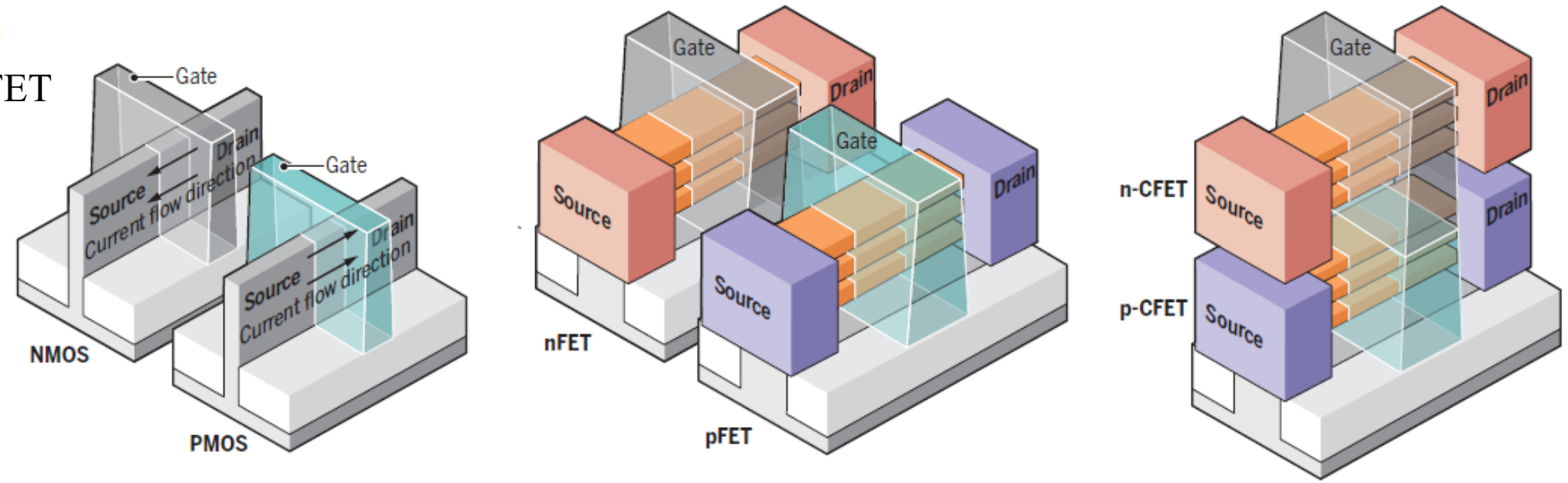
Imaging the metal-interconnect *connectome* in Intel technology

Chip Scan: 3D X-ray image of Intel Pentium G3260 processor manufactured in 22 nm FinFET technology





FinFET



"16 nm" technology node, ~30 transistors per μm^2

[Toward attojoule switching energy in logic transistors | Science]

Detail of FinFET CMOS technology

Design: 3D image of typical CMOS design

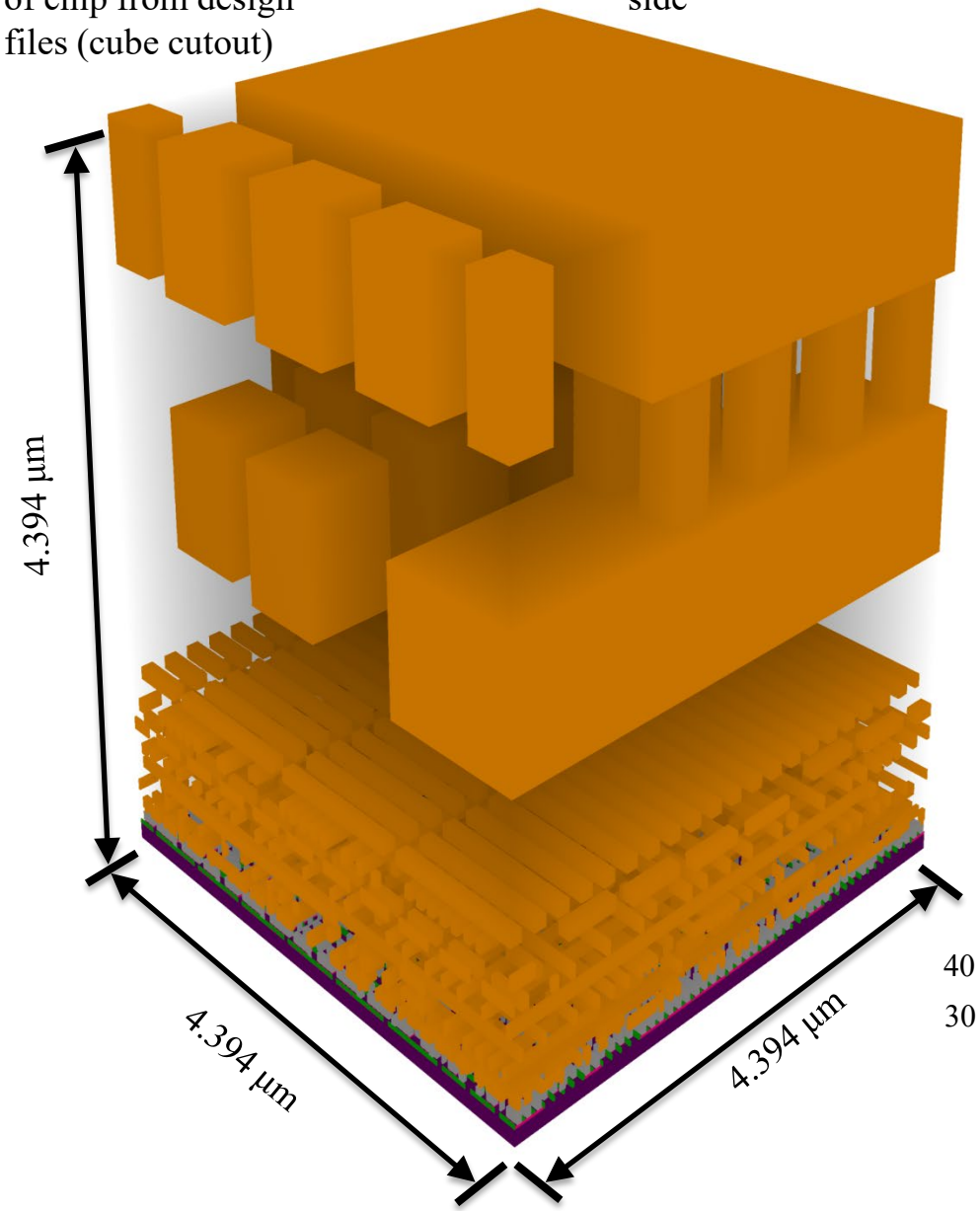
$n_{index} = 1 - \delta + i\beta$

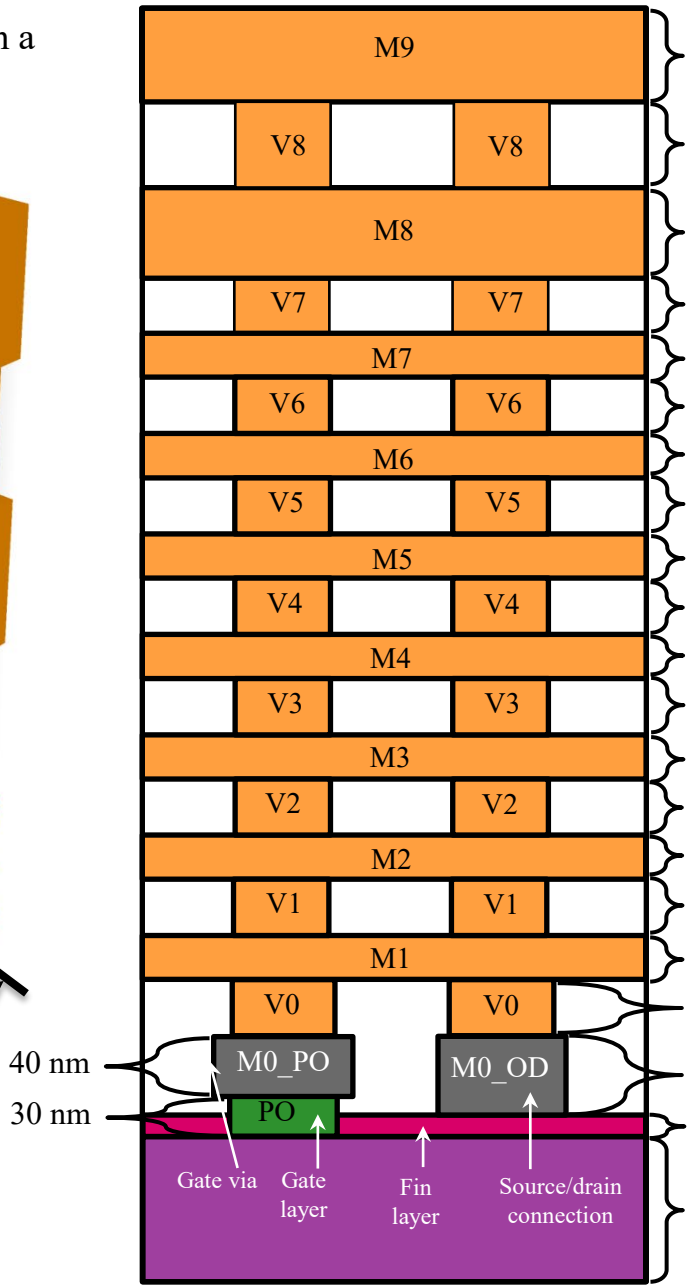
Plane wave propagation $e^{in_{index}kx}$

Material Legend	n_{index} values (x 10^{-6})	E = 6.2 keV (λ = 0.2 nm) PSI light source
SiO_2	δ	12.061
	β	0.257
	1/α (μm)	61.827
Si	δ	12.847
	β	0.478
	1/α (μm)	33.295
Al	δ	14.358
	β	0.431
	1/α (μm)	36.945
W	δ	79.706
	β	9.841
	1/α (μm)	1.617
Cu	δ	42.636
	β	1.480
	1/α (μm)	10.756

3D volume rendering of chip from design files (cube cutout)

Voxel size is 5 nm on a side

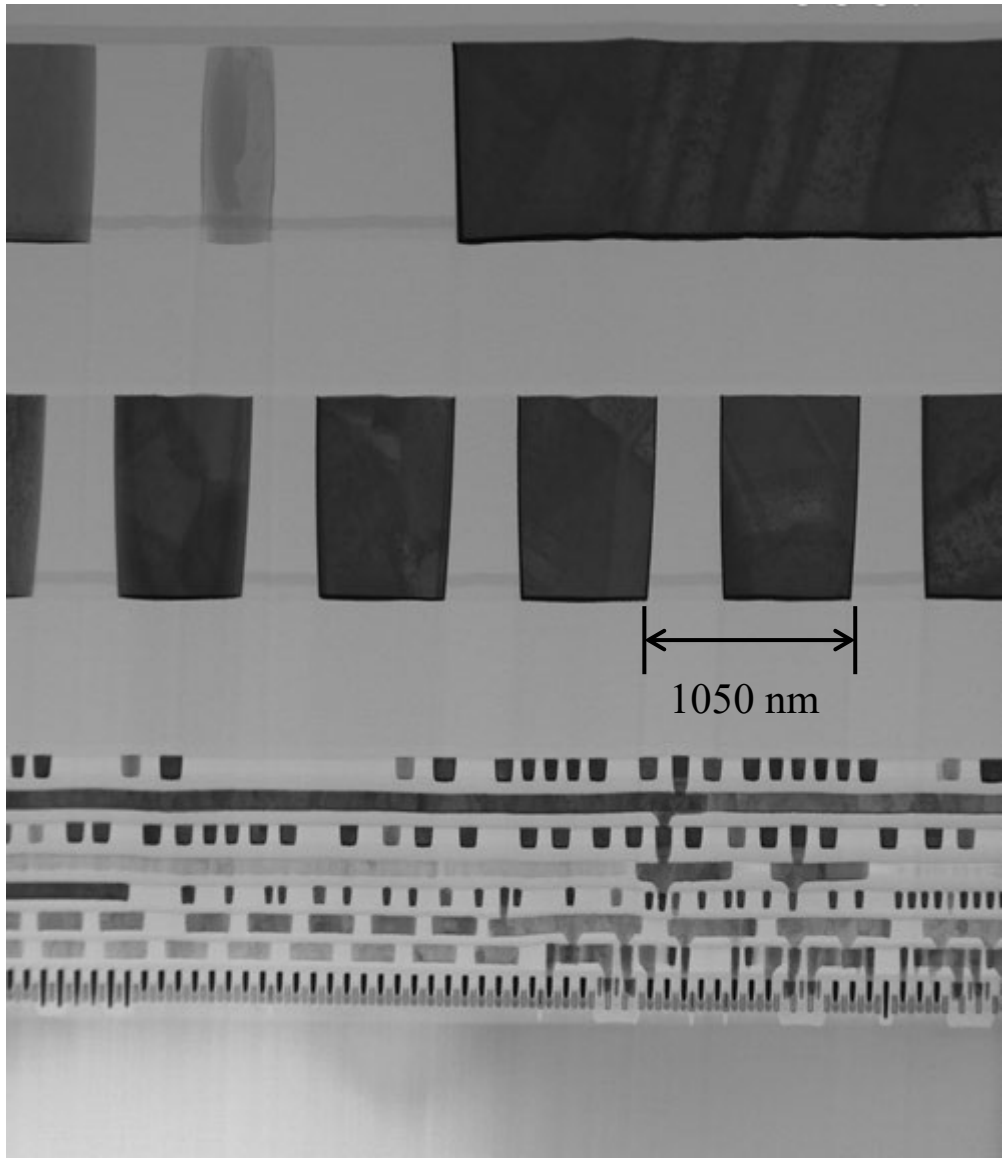




Nominal layer thicknesses

850 nm
800 nm
850 nm
800 nm
80 nm
68 nm
80 nm
63 nm
80 nm
63 nm
70 nm
63 nm
70 nm
60 nm
70 nm
60 nm
70 nm
27 nm
54 nm
16 nm
Substrate: 100 nm

Example TEM cross-section to determine layer thicknesses of manufactured CMOS chip



M9, 778 nm

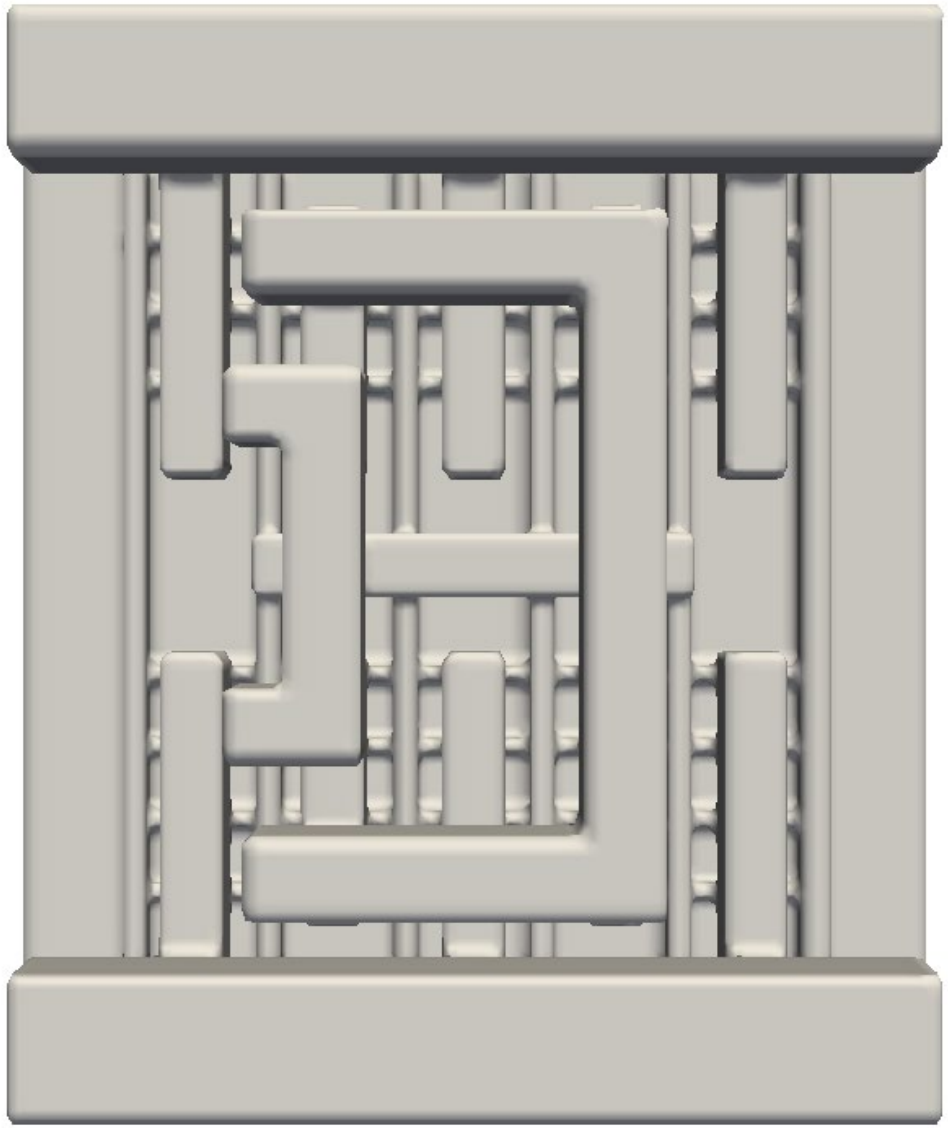
V8, 620 nm

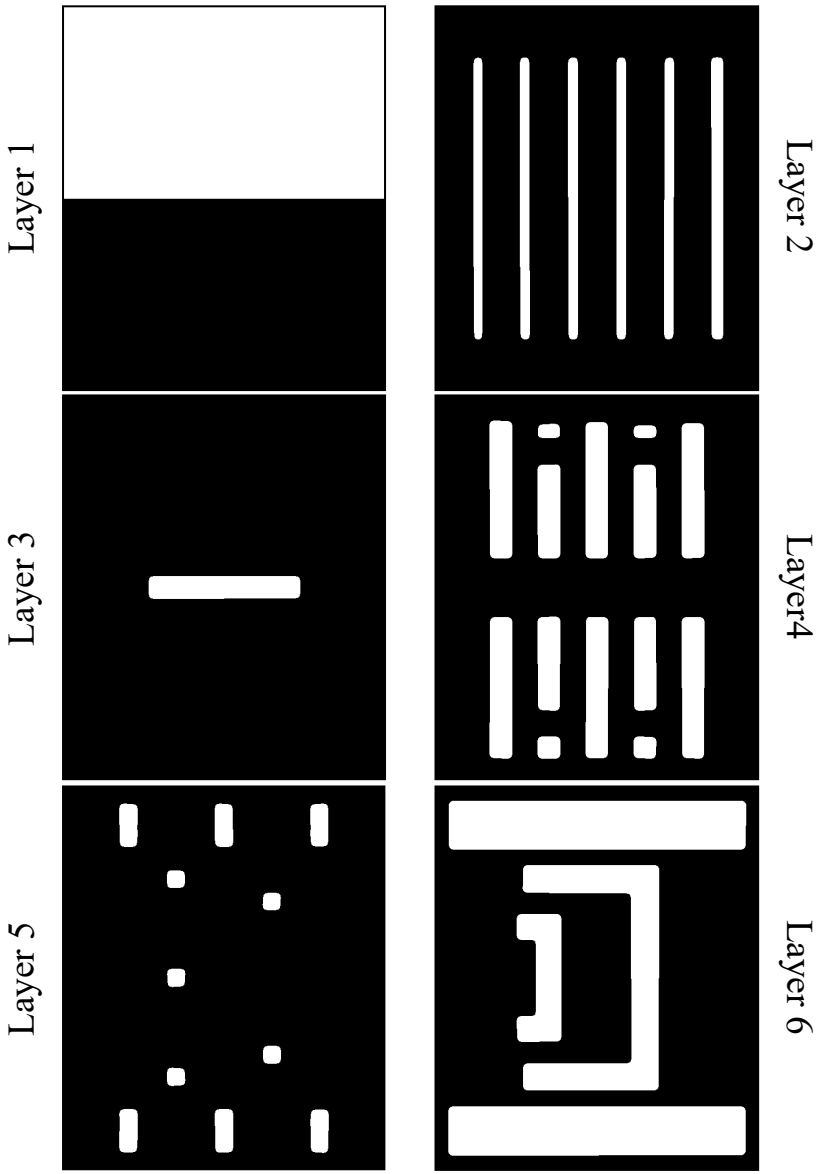
M8, 809 nm

V7, 626 nm

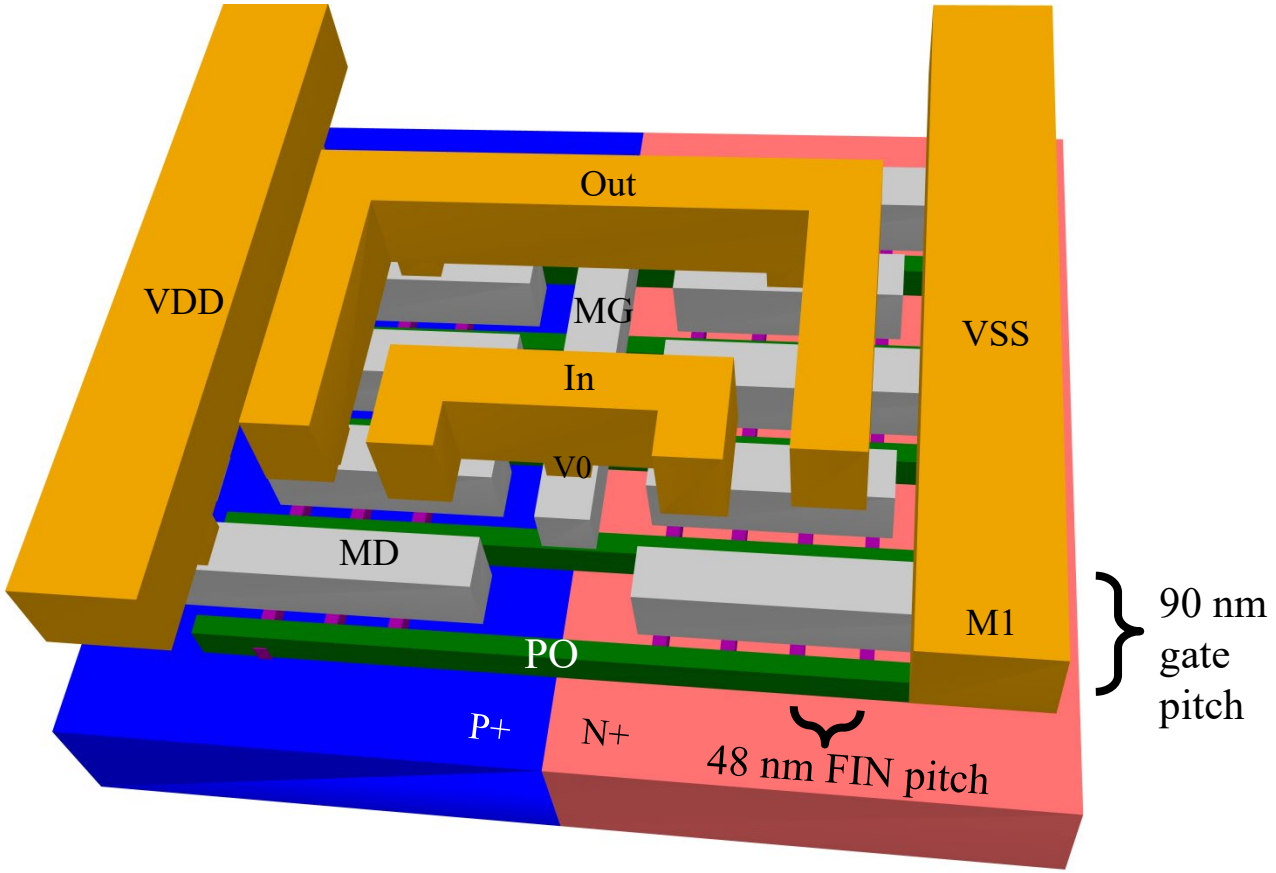
M7, 89 nm
V6, 42 nm
M6, 87 nm
V5, 49 nm
M5, 90 nm
V4, 55 nm
M4, 75 nm
V3, 35 nm
M3, 70 nm
V2, 40 nm
M2, 75 nm
V1, 45 nm
M1, 75 nm

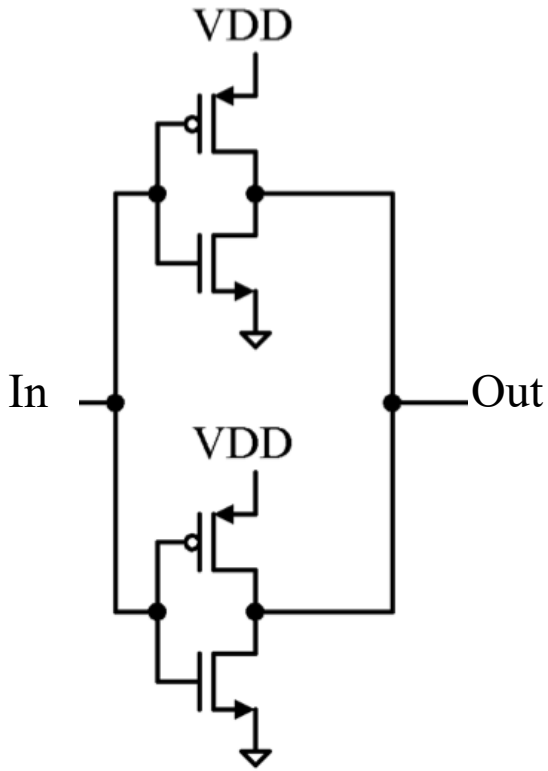
Example: 3D transistor circuit structures from 2D photolithographic mask design





Example: 3D image and schematic of inverter circuit *design* in CMOS FinFET technology



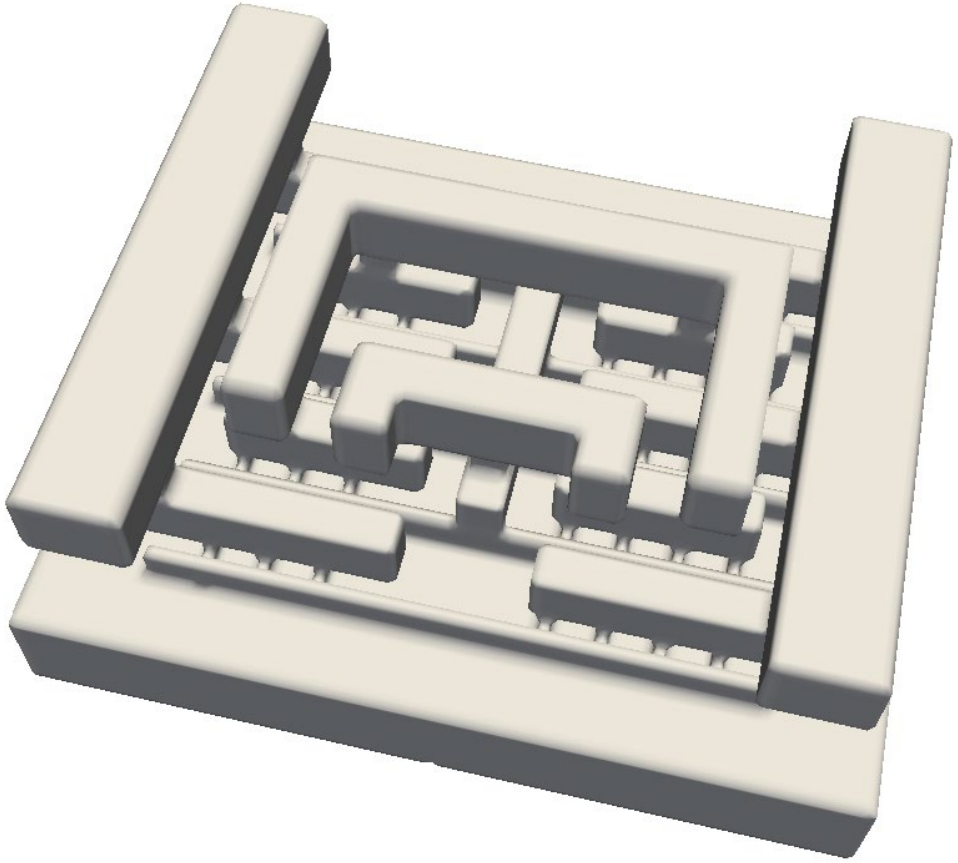


Name	Thickness	Material	Function
FIN	0.016	Si	Fin, n+/p+ diffused regions, 10 nm width, 48 nm pitch
PO	0.030	Al/TiN	Metal gate conductor, 16 nm width, 90 nm pitch
MG	0.040	W	Connect PO to M1 thru V0
MD	0.054	Silicide	Connect drain/source to M1 thru V0
V0	0.027	Cu	Via connecting MG, MD to M1
M1	0.070	Cu	First-level 1x metal line

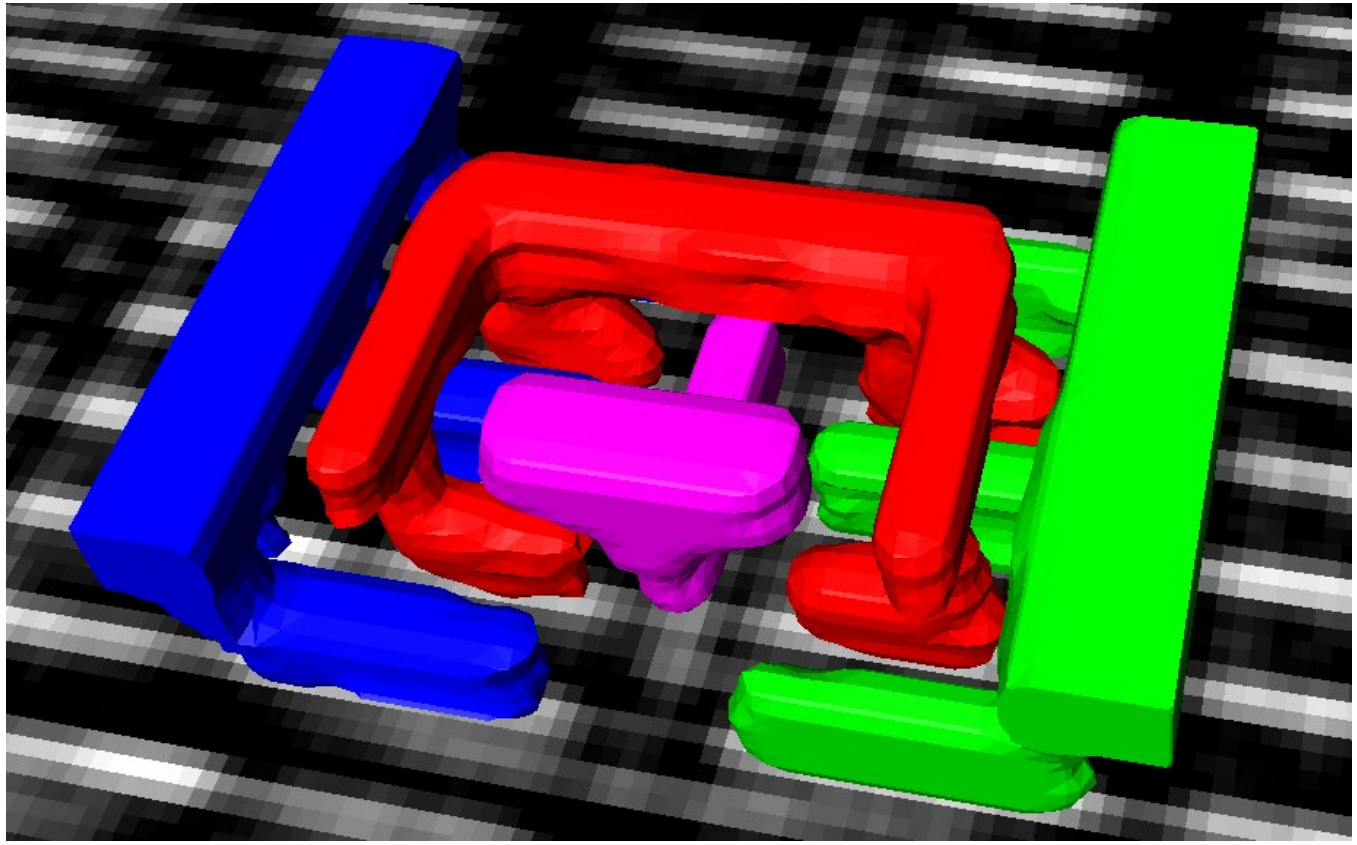
Inverter
Gate: Pitch = 90 nm, width = 16 nm
Fin: Pitch = 48 nm, width = 10 nm
Volume: 666 nm x 556 nm x 267 nm

Comparison of *design* and 3D X-ray image of *manufactured* circuit element

CMOS FinFET inverter *design* in 16 nm technology



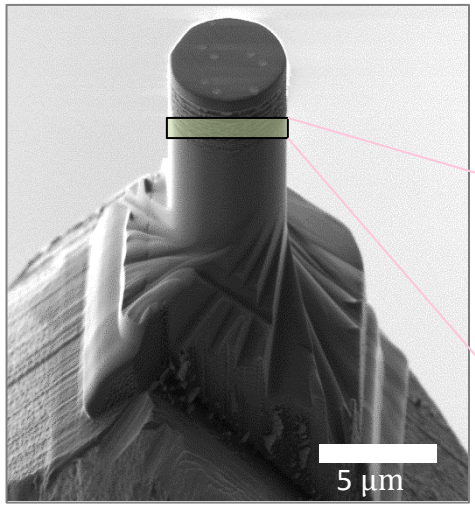
3D-image of manufactured CMOS FinFET inverter (2018)
Published: M. Holler et al., *Nature Electronics* **2**, 464 (2019)



Gate: Pitch = 90 nm, width = 16 nm
Fin: Pitch = 48 nm, width = 10 nm
Volume: 666 nm x 556 nm x 267 nm

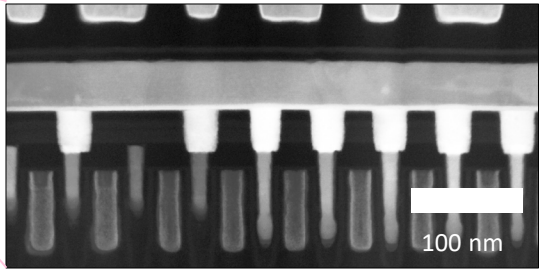
Closing the resolution gap between TEM cross-sections and 3D X-ray imaging

Published: T. Aidukas et al., *Nature* **632**, 81 (2024)



Integrated circuit sample (FIB cutout from chip)

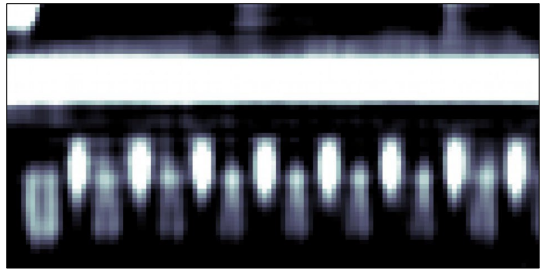
Transmission electron microscopy



Sub-nm resolution in very small volume cross-section. The lamella is precisely cut out of bulk chip using a Focused Ion Beam (FIB)

Resolution gap

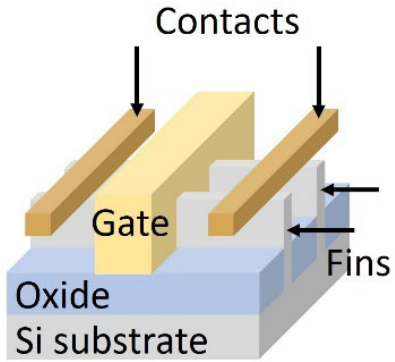
3D X-ray microscopy

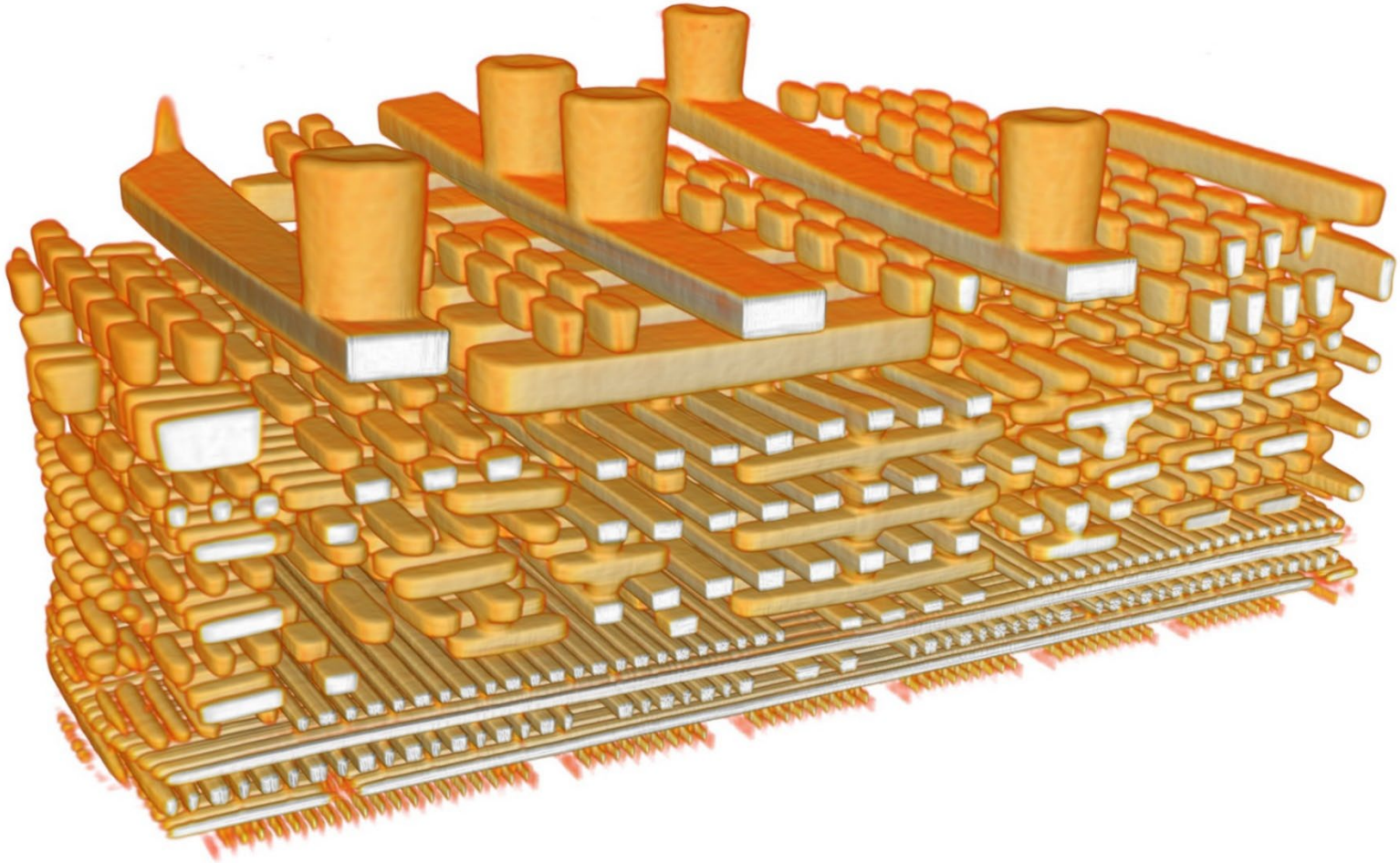


4-nm resolution in bulk 3D volume of chip obtained from X-ray imaging and without damaging the sample

Non-destructive 3D X-ray imaging of integrated circuits at 4 nm resolution

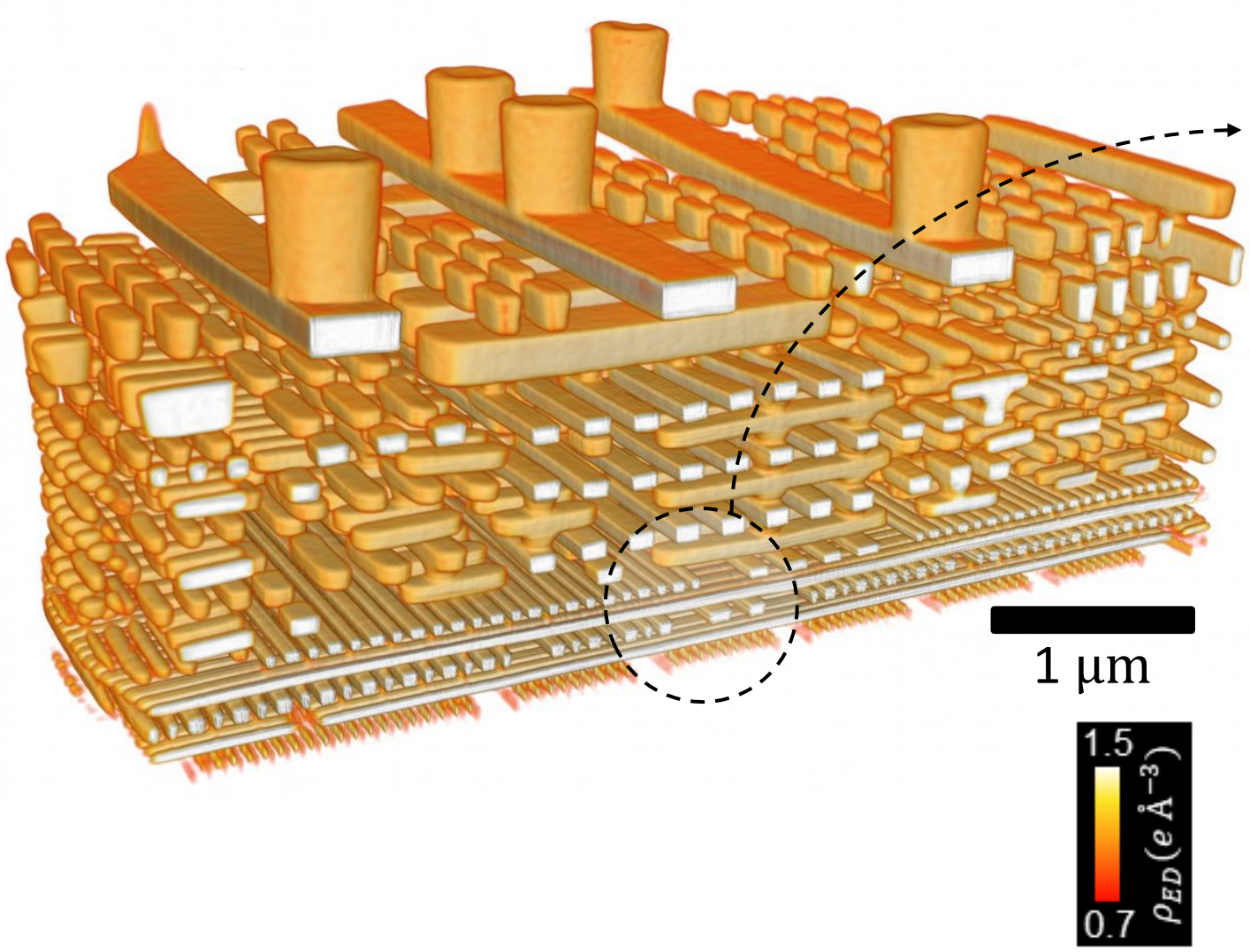
- Published: T. Aidukas et al.,"High-performance 4 nm resolution X-ray tomography using burst ptychography", *Nature* **632**, 81 (2024), https://rdcu.be/dPAzd

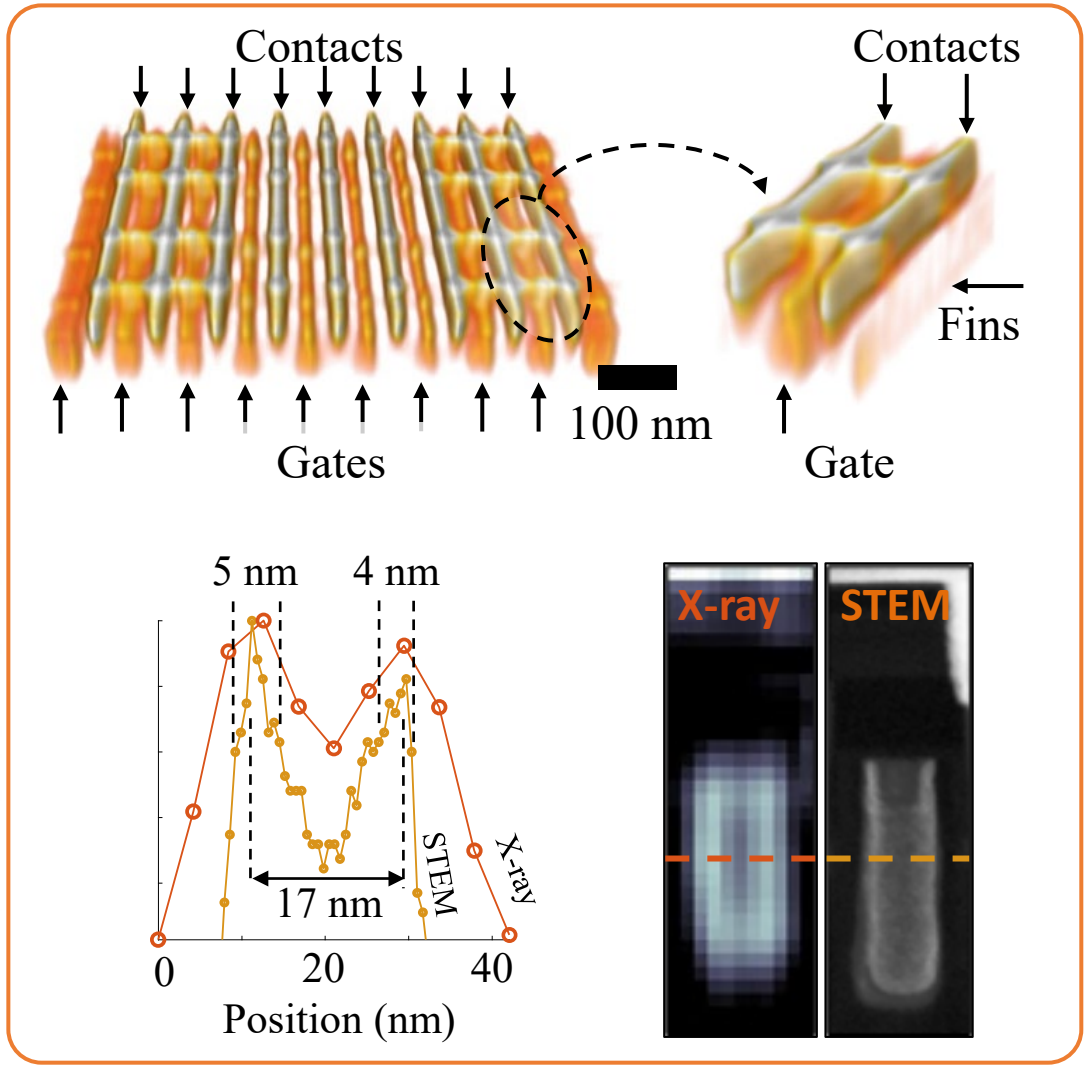




- 4 nm resolution in 3D with path to sub-1 nm
- 5 µm depth of field with filtered backpropagation
- Example 3D X-ray image of metal interconnect (connectome) and transistors in AMD Ryzen 5 5600G Processor with TSMC 7 nm technology

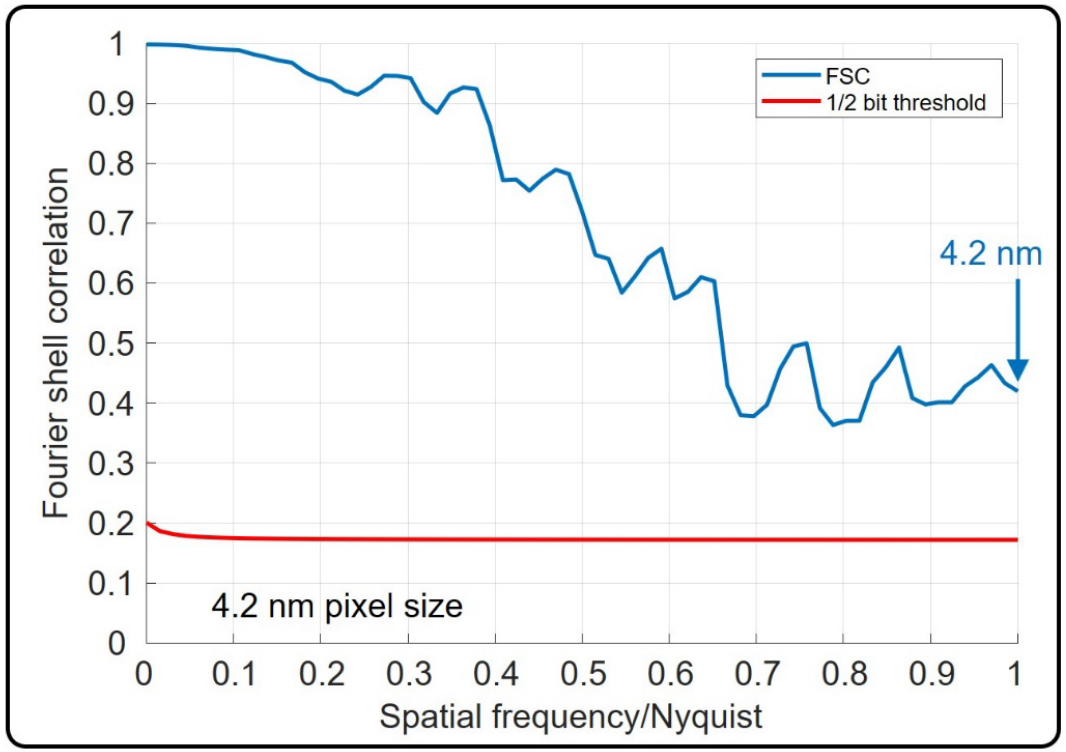
Non-destructive 3D X-ray imaging of integrated circuits at 4 nm resolution

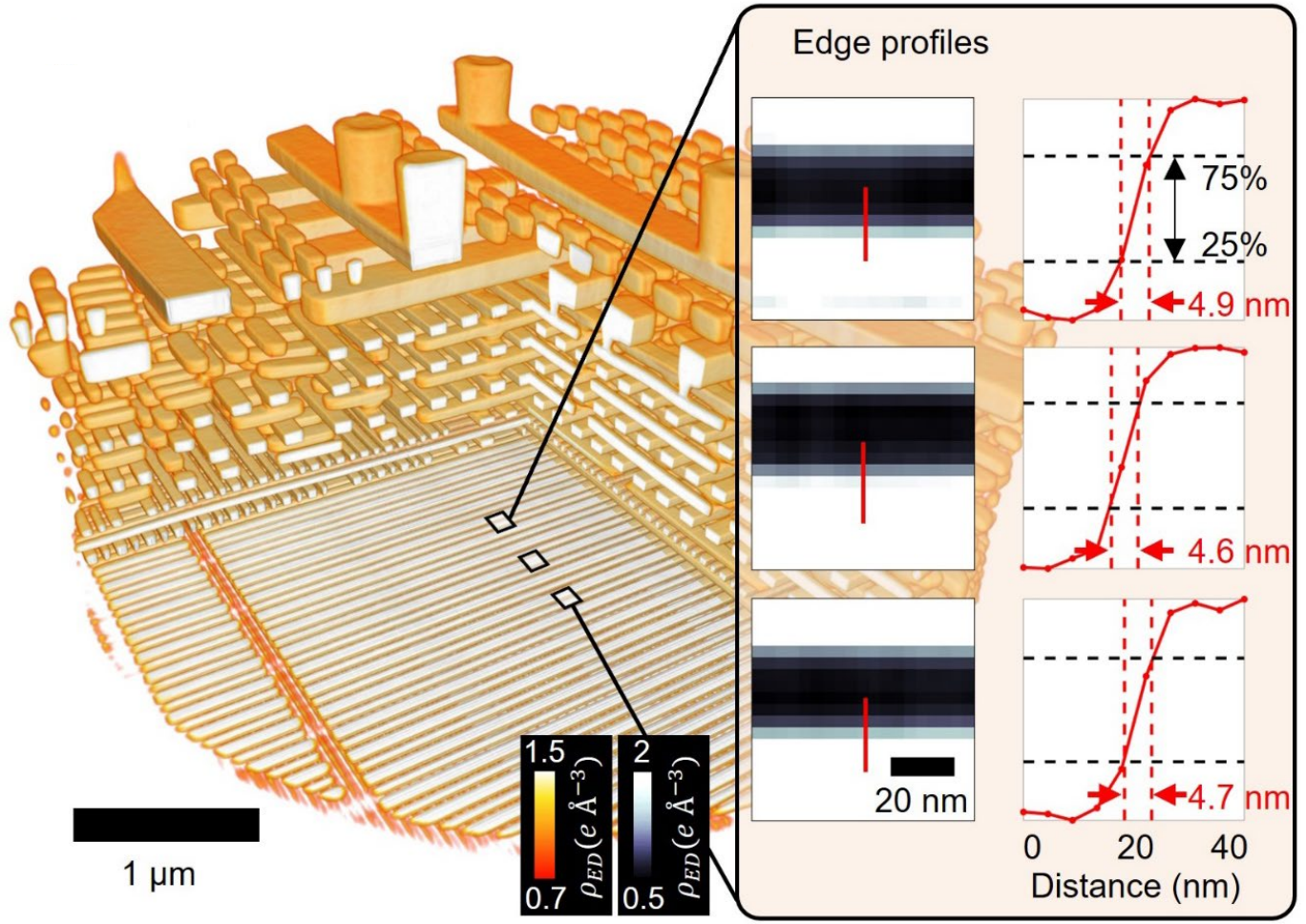




Non-destructive 3D X-ray imaging of integrated circuits at 4 nm resolution

Fourier shell correlation analysis and edge profiles

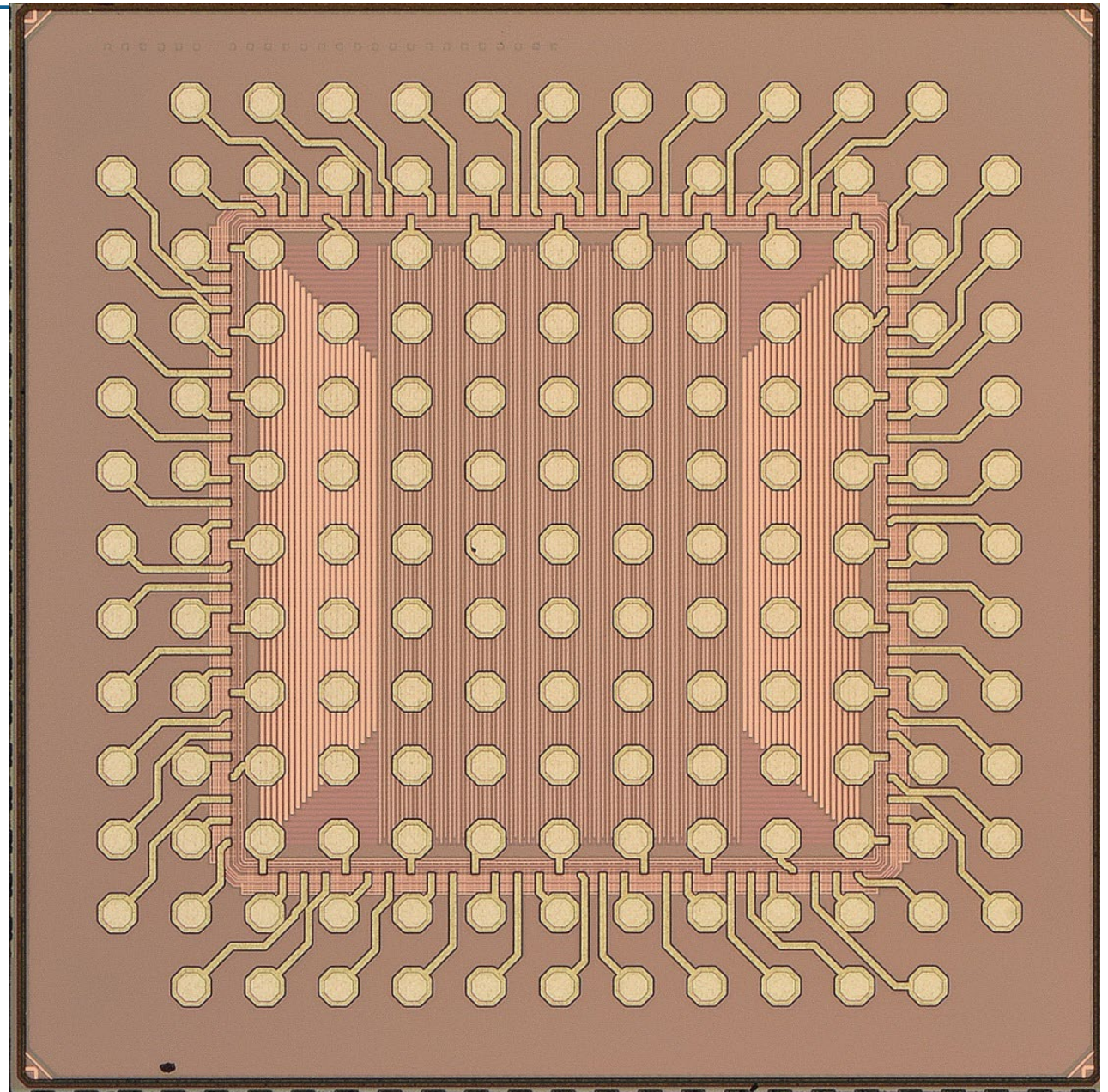




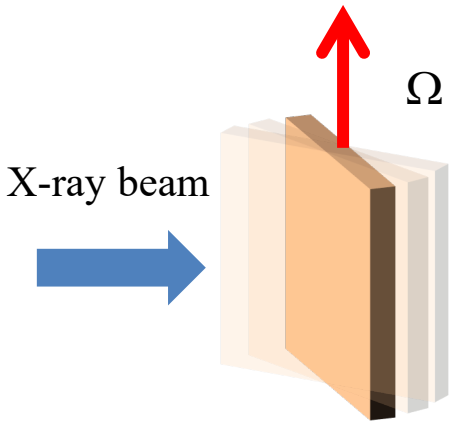
Large-area 3D X-ray imaging of CMOS chips

The need for large-area, lensless, 3D coherent X-ray imaging geometry with zoom capability

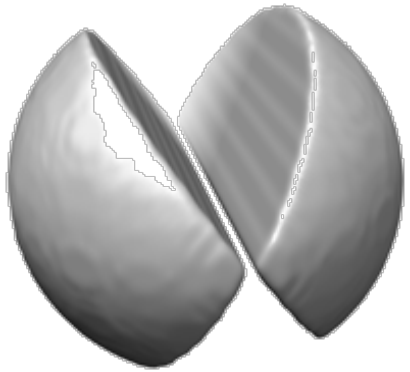
- Optical photograph of typical CMOS test die – in this case, an encryption engine implemented in a 16nm FinFET technology
- 2.5 x 2.5 mm^2 area
- 13 x 13 – 4 = 165 solder bump pads
- 170 µm pitch, 89.04 µm diameter, 80.96 µm space



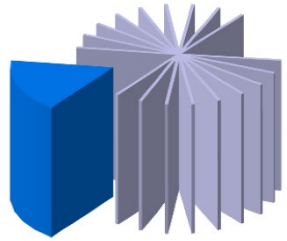
Sample geometry for large-area chip scan: The challenge of missing information with limited-angle X-ray tomography and laminography

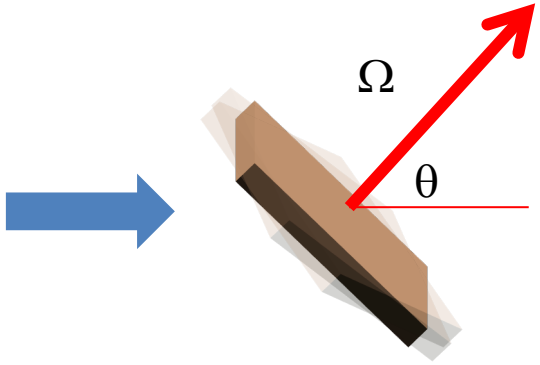


Limited-angle tomography at normal incidence and limited rotation Ω about chip-plane

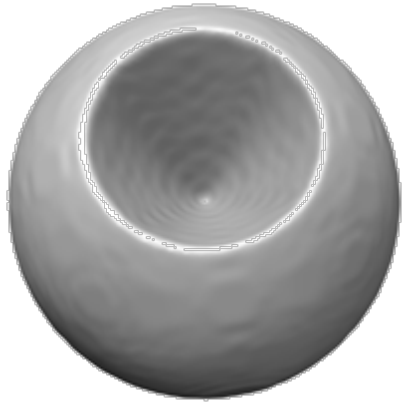


Missing *wedge* in 3D diffraction data

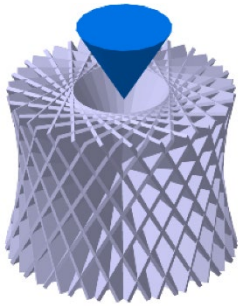




Laminography at angle θ and rotation Ω about chip-normal



Missing *cone* in 3D diffraction data



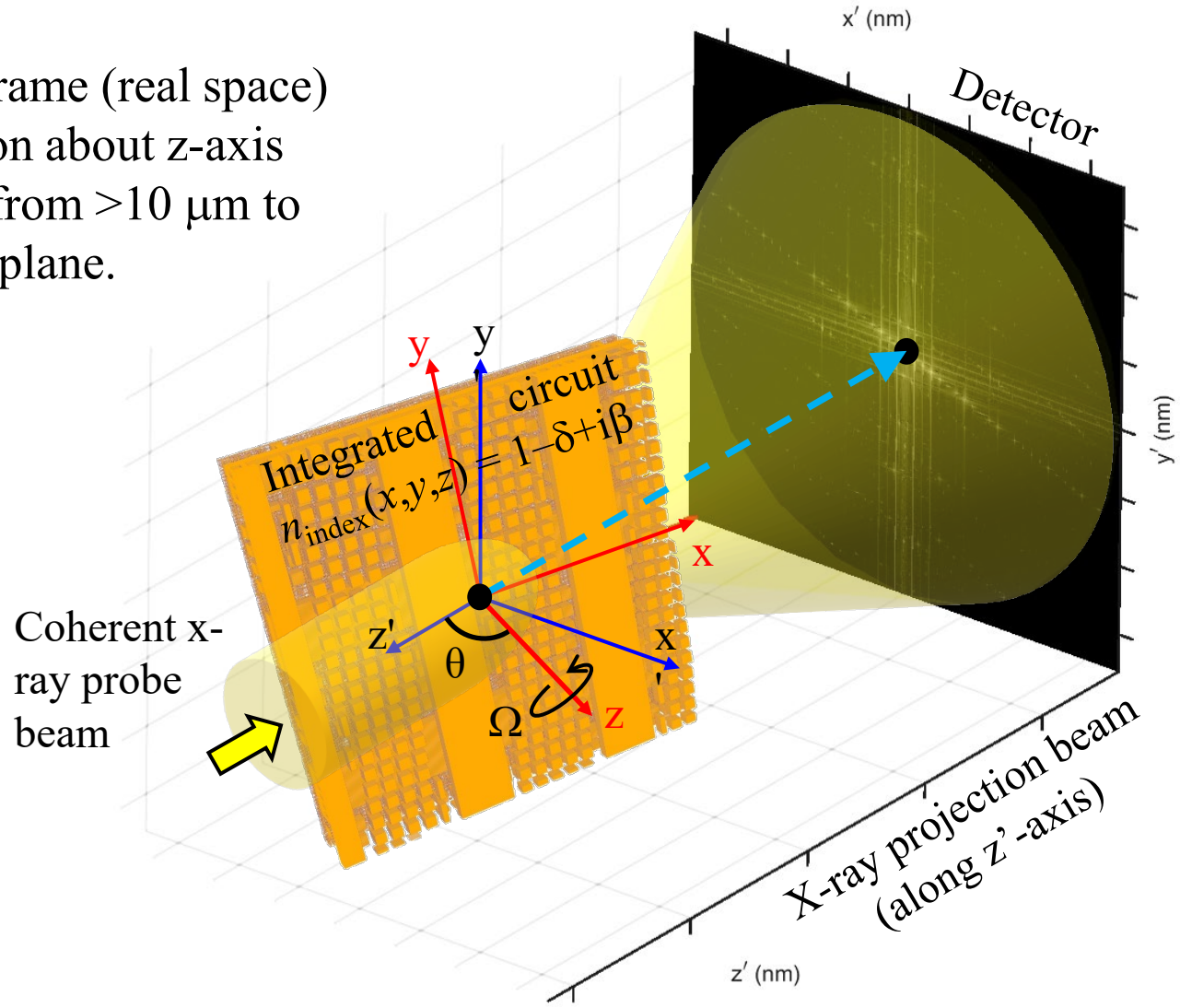
- Tomography at normal incidence suffers from reconstruction artifacts due to the missing wedge of diffraction data (missing information)
- The laminography geometry is suitable for flat samples such as integrated circuits (ICs) and the missing cone is less data lossy than the missing wedge of diffraction data in standard tomography

Sample geometry for large-area chip scan explored using chip design data

Laminography geometry: probe-beam reference frame (real space) (Tilt angle from chip-plane normal θ = 61°, rotation about z-axis Ω = 0°:1°:359°). Probe-beam diameter selectable from >10 μm to <1 μm. Integrated circuit is ~7.3 m from detector plane.

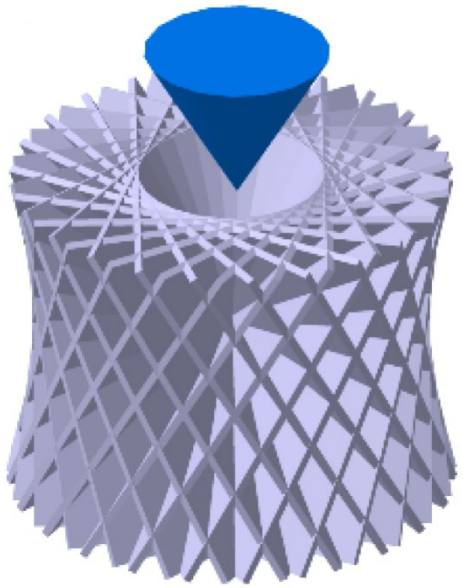
The 2D Fourier transform $P(k_u, k_v)$ of a projection through the sample corresponds to a cross-section of the 3D Fourier transform $M(k_x, k_y, k_z) = FT\{n_{index}(x, y, z)\}$.

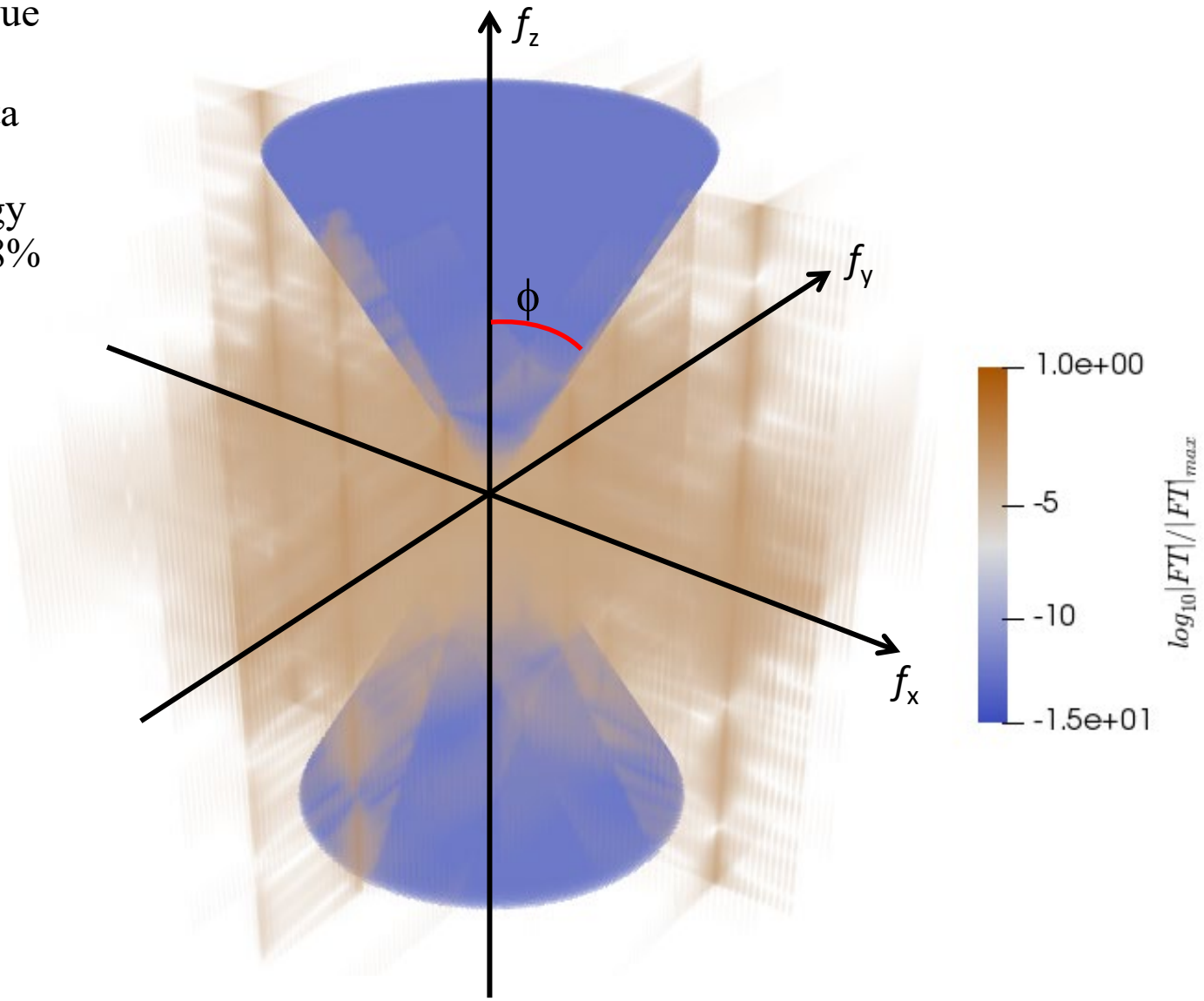
The vectors k_u and k_v span a Cartesian coordinate system on this plane.



Missing cone in laminography chip design diffraction data

- Laminography null space is blue cone ($\theta = 61°$, $\phi = 29°$)
- Missing volume = 8.0% in data cube
- Example spatial spectral energy removed from structure = 23.8%

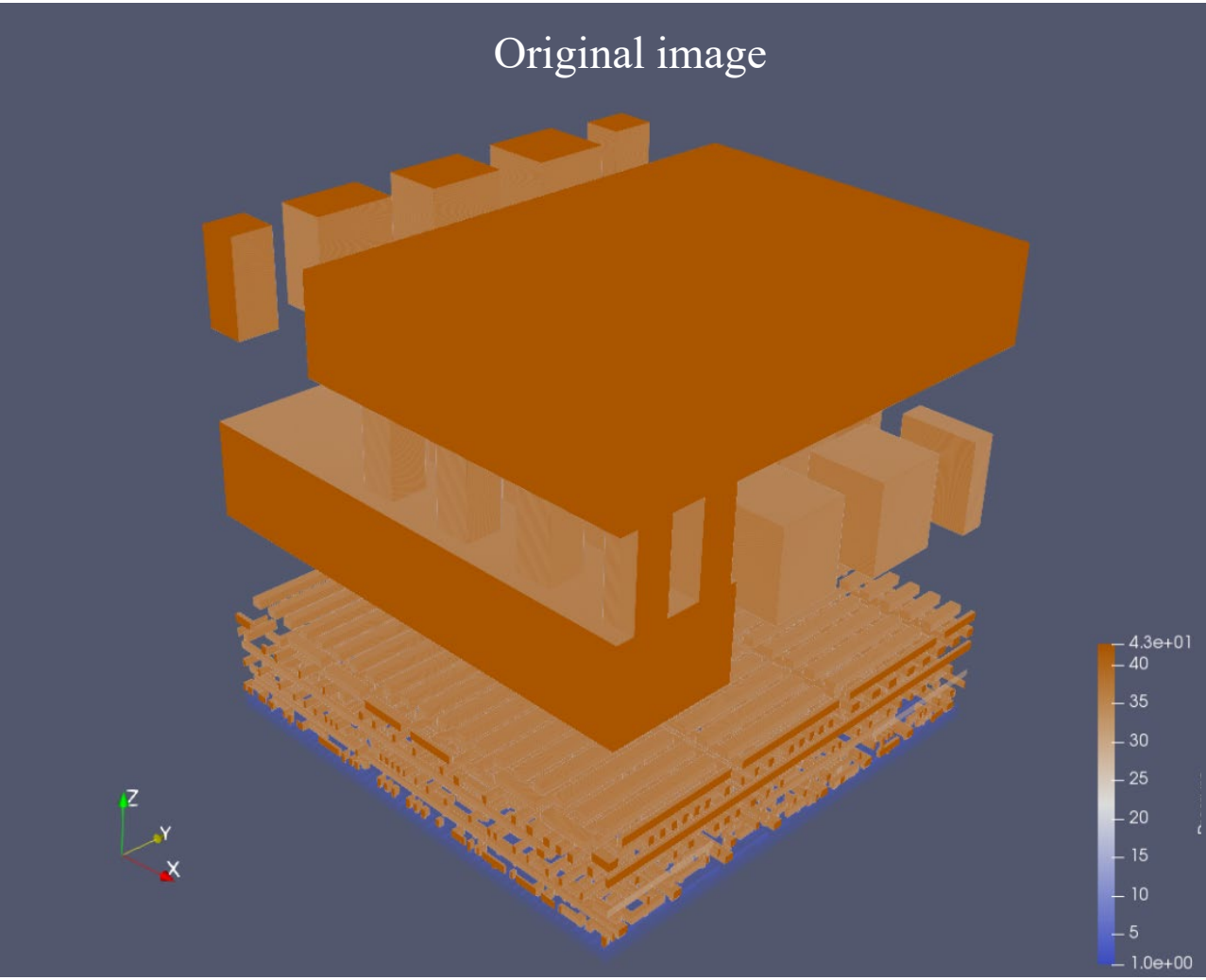




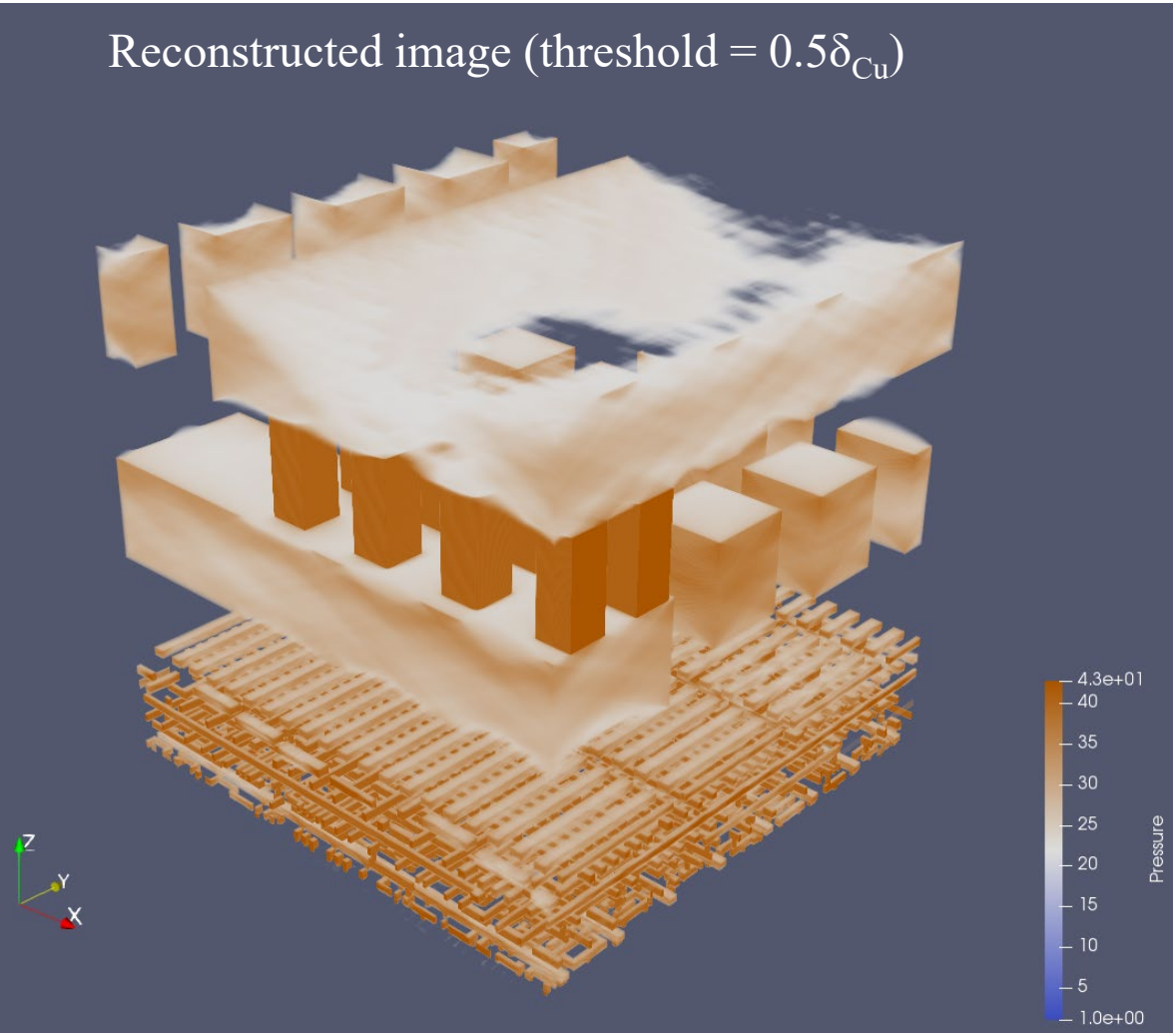
Impact on image reconstruction of missing cone in diffraction data

Laminography with $\theta = 61^{o}$ and missing cone

Original image



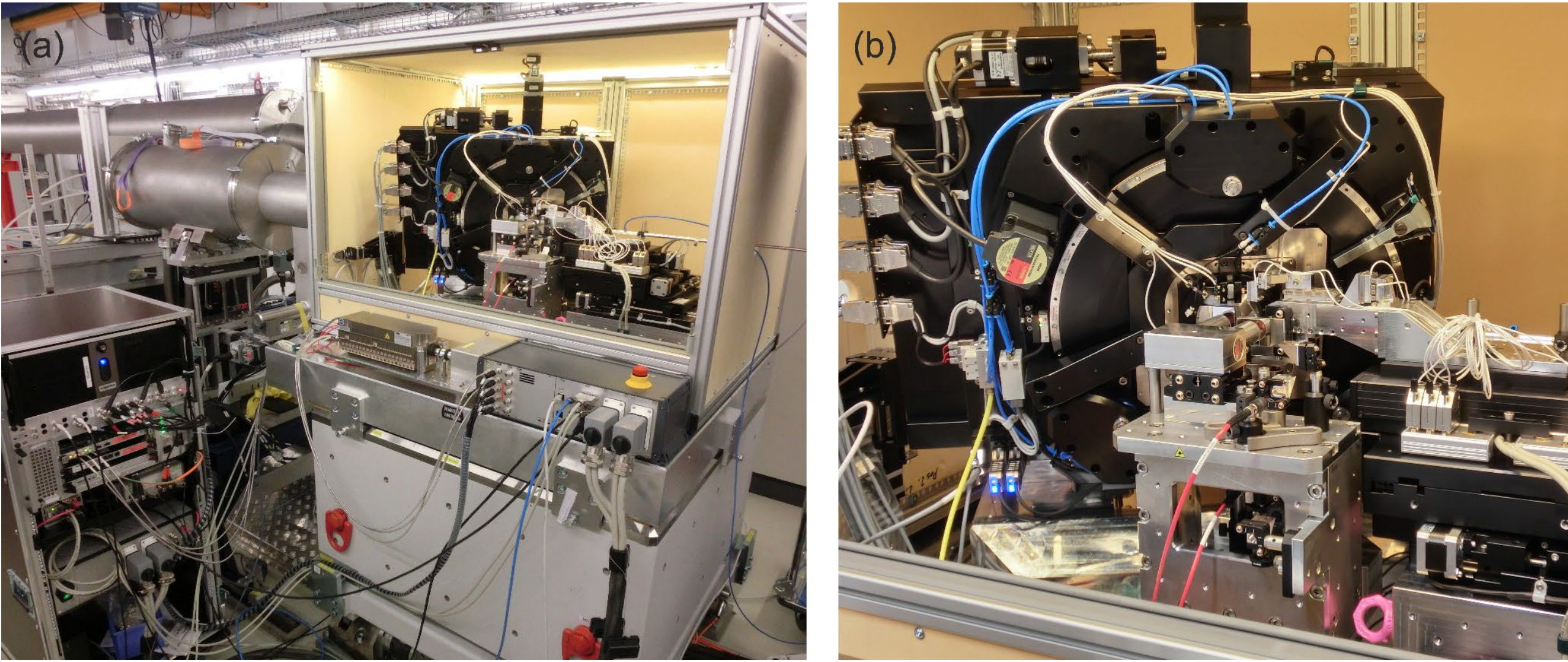
Reconstructed image (threshold = $0.5\delta_{Cu}$)



Materials: SiO_2, Si, W, Al, Cu

Design, construction, and demonstration of Laminography Microscope

3D x-ray chip-scan microscope (2018 beta-version, now at ANL)

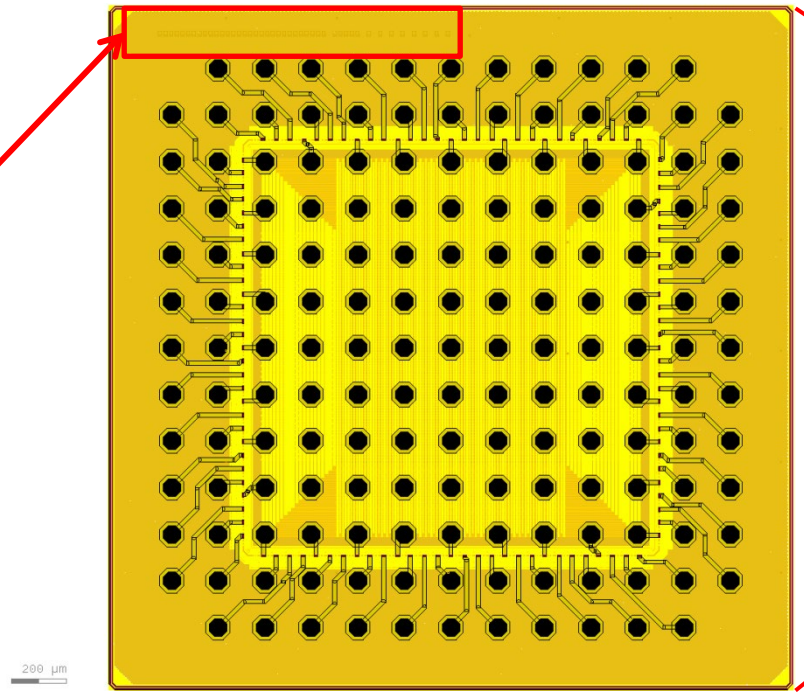


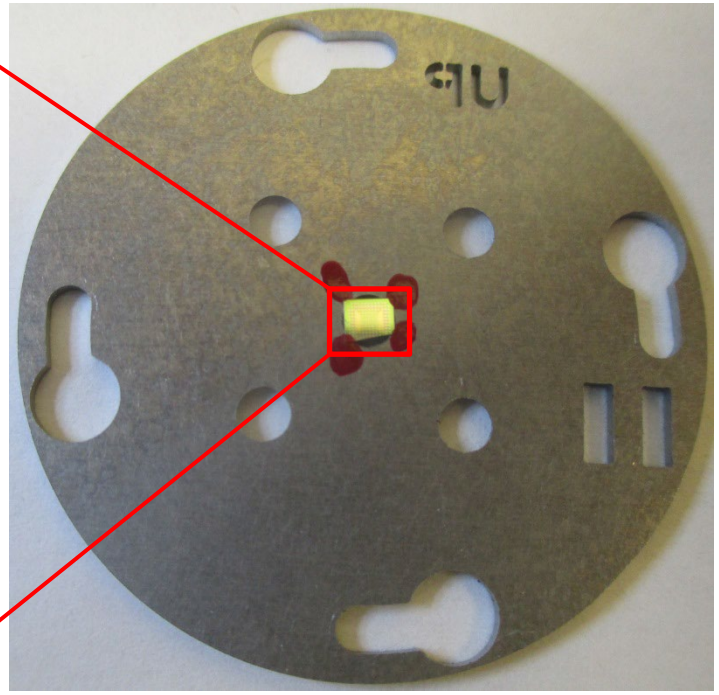
Laminography microscope at SLS cSAXS beamline with enclosure doors removed. (a) Overview with flight tube and control rack. (b) Stage detail

Sample preparation for large-area, lensless, 3D coherent X-ray imaging

Chip orientation

Top left-hand side of chip





16nm FinFET technology CMOS FF+

2.5x2.5 mm^2 chip area, 0.9x0.9 mm^2 circuit area

13x13–4=165 solder bump pad. No solder balls.

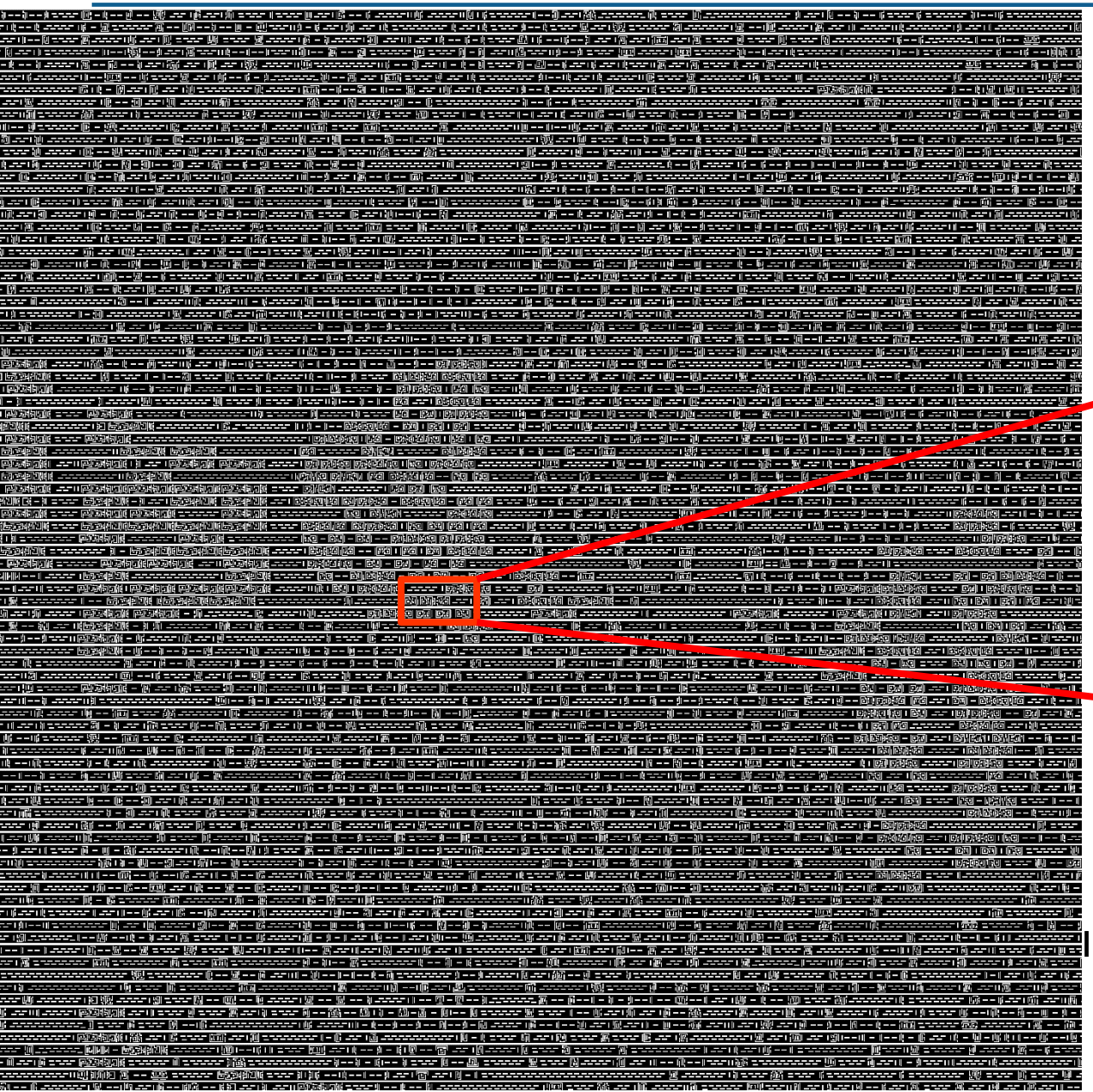
170 µm pitch, 89.04 µm diameter, 80.96 µm space

Silicon substrate thickness 20 µm after thinning

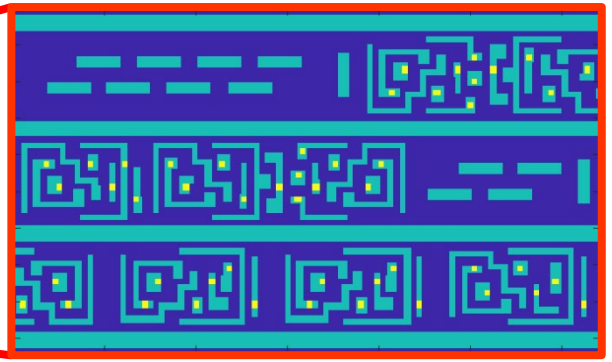
Total thickness 25 µm

Chip mounted on Laminography holder using red nail polish (!) and photographed in gel pack. Chip orientation as indicated and facing camera.

Keeping track of circuit design and imaged layers

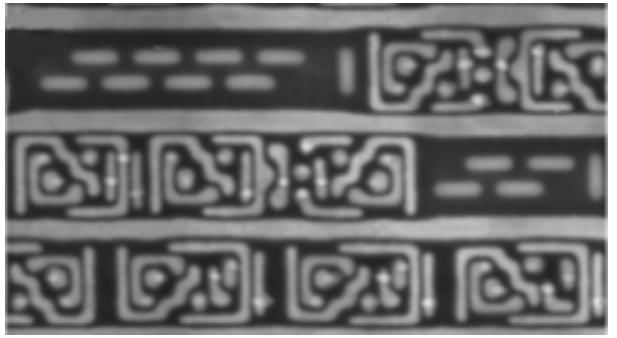


M1 and V1 mask



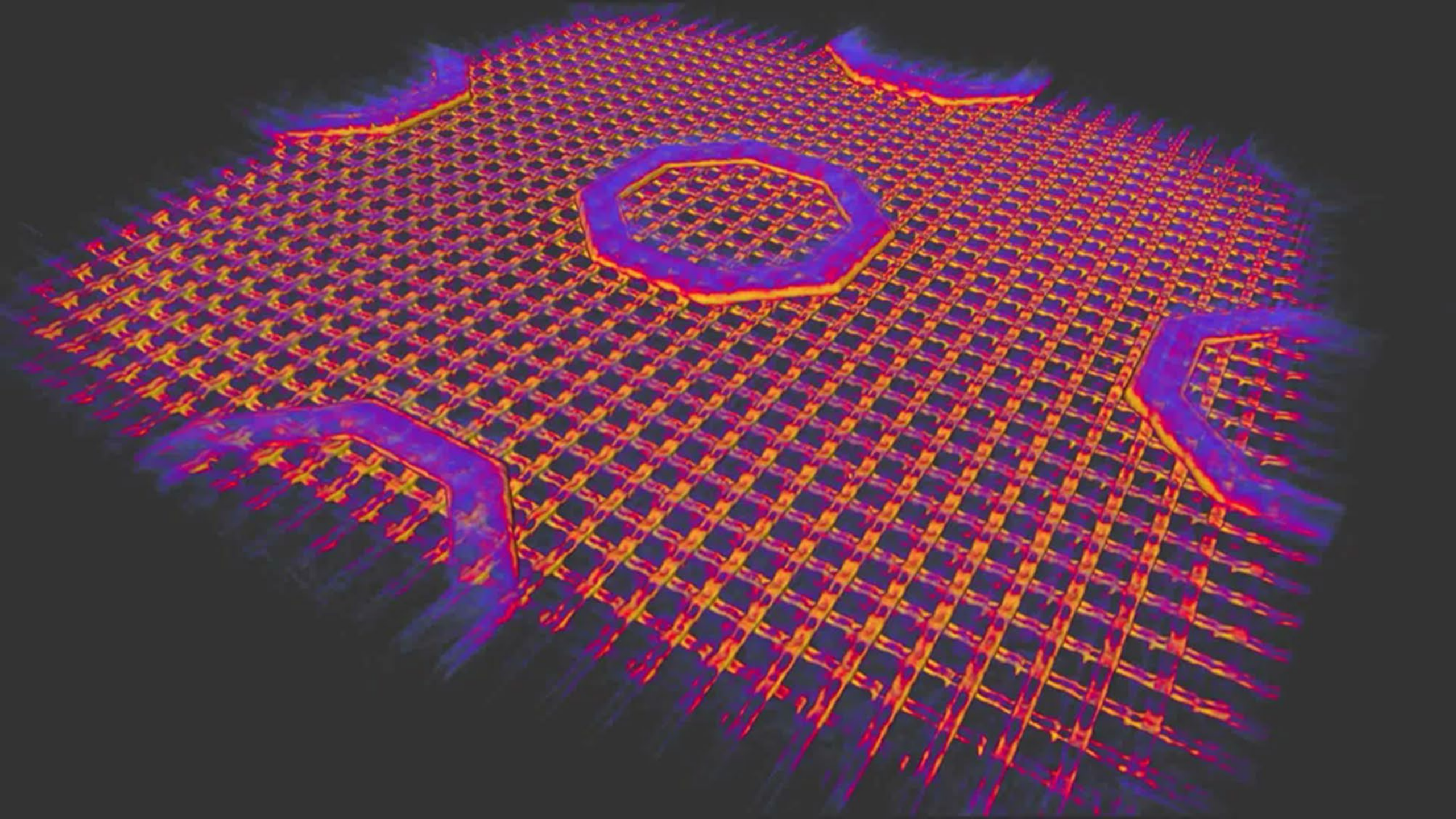
1 µm

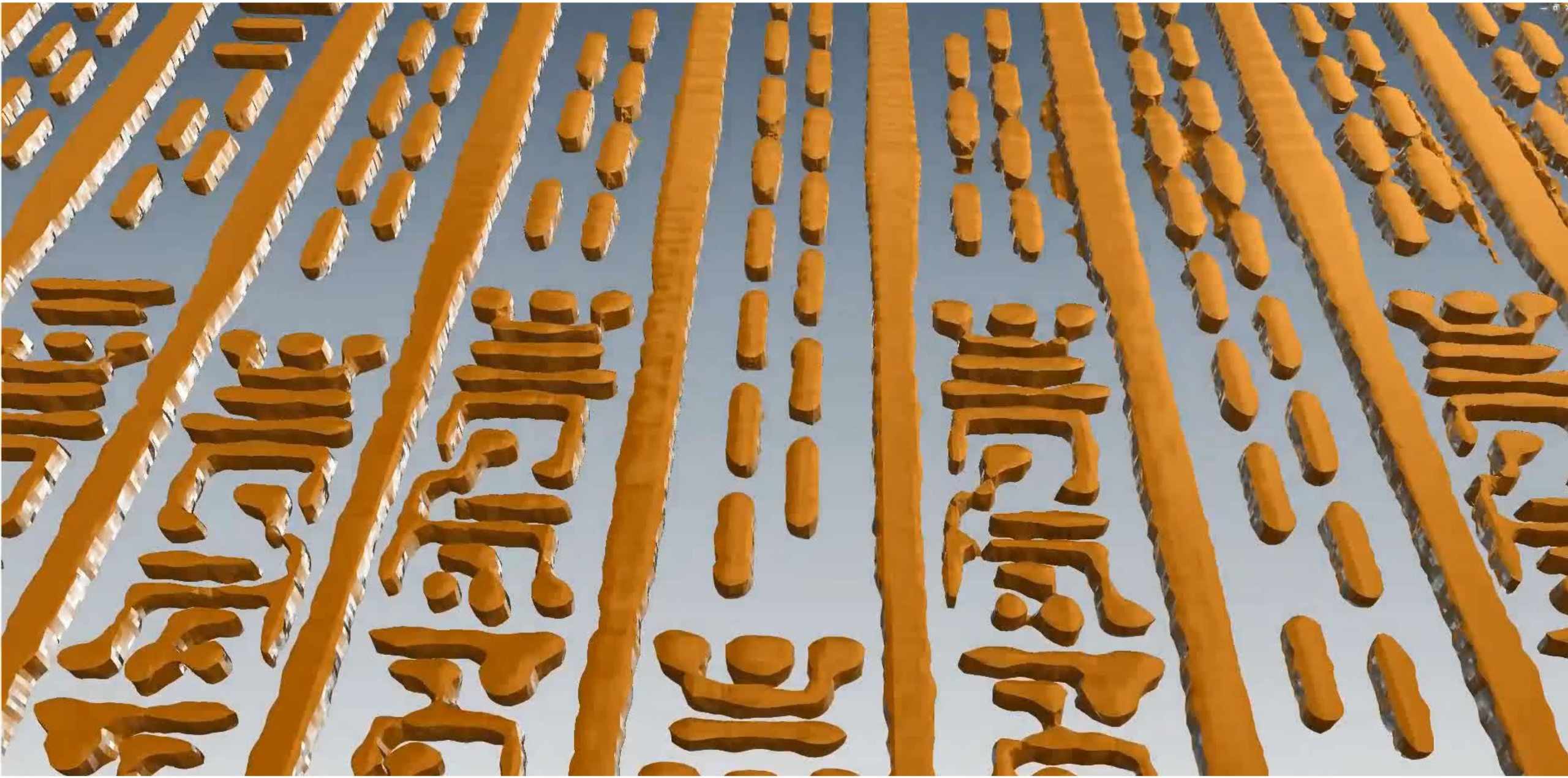
SEM image

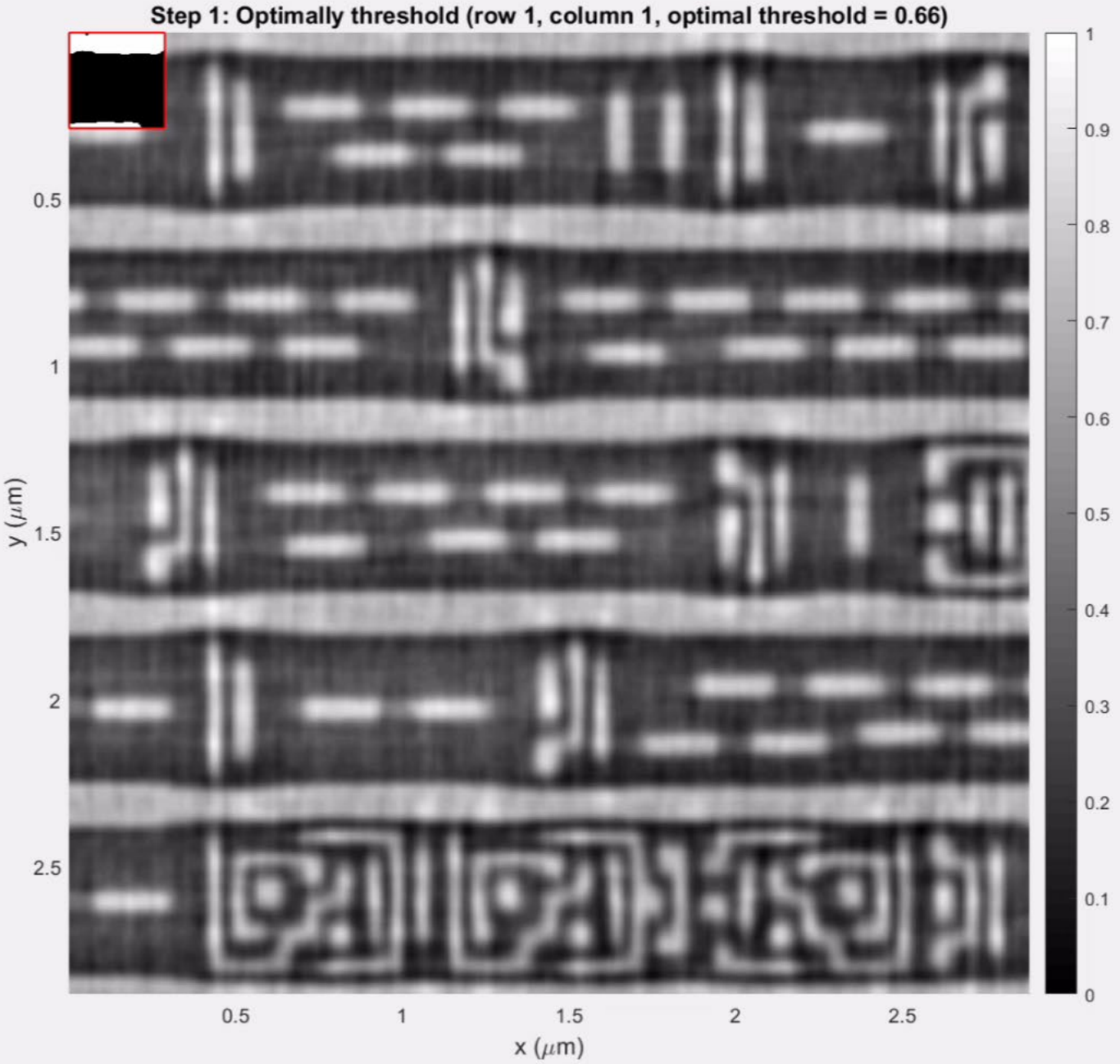


1 µm

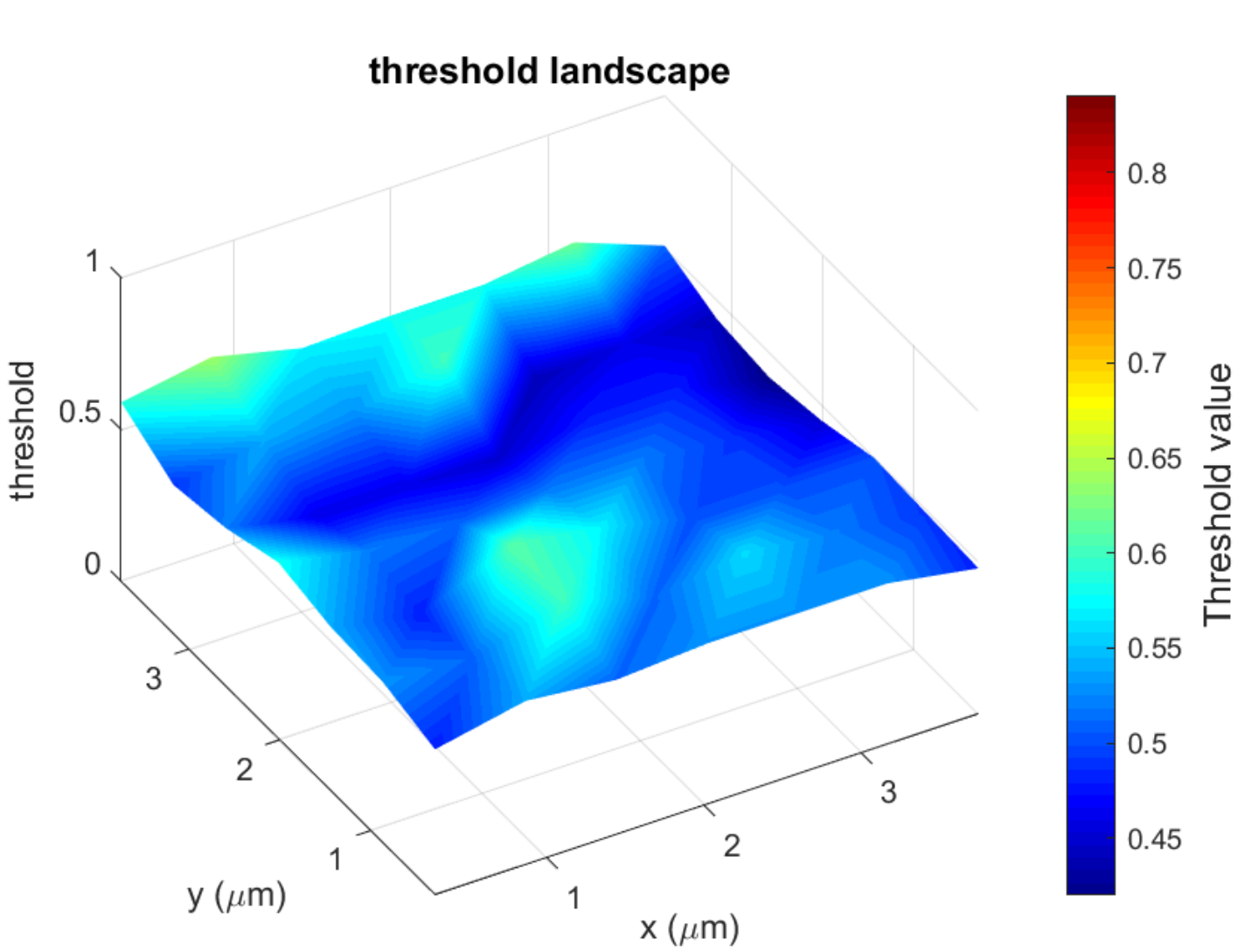
3D X-ray imaging and non-destructive virtual delayering of chip

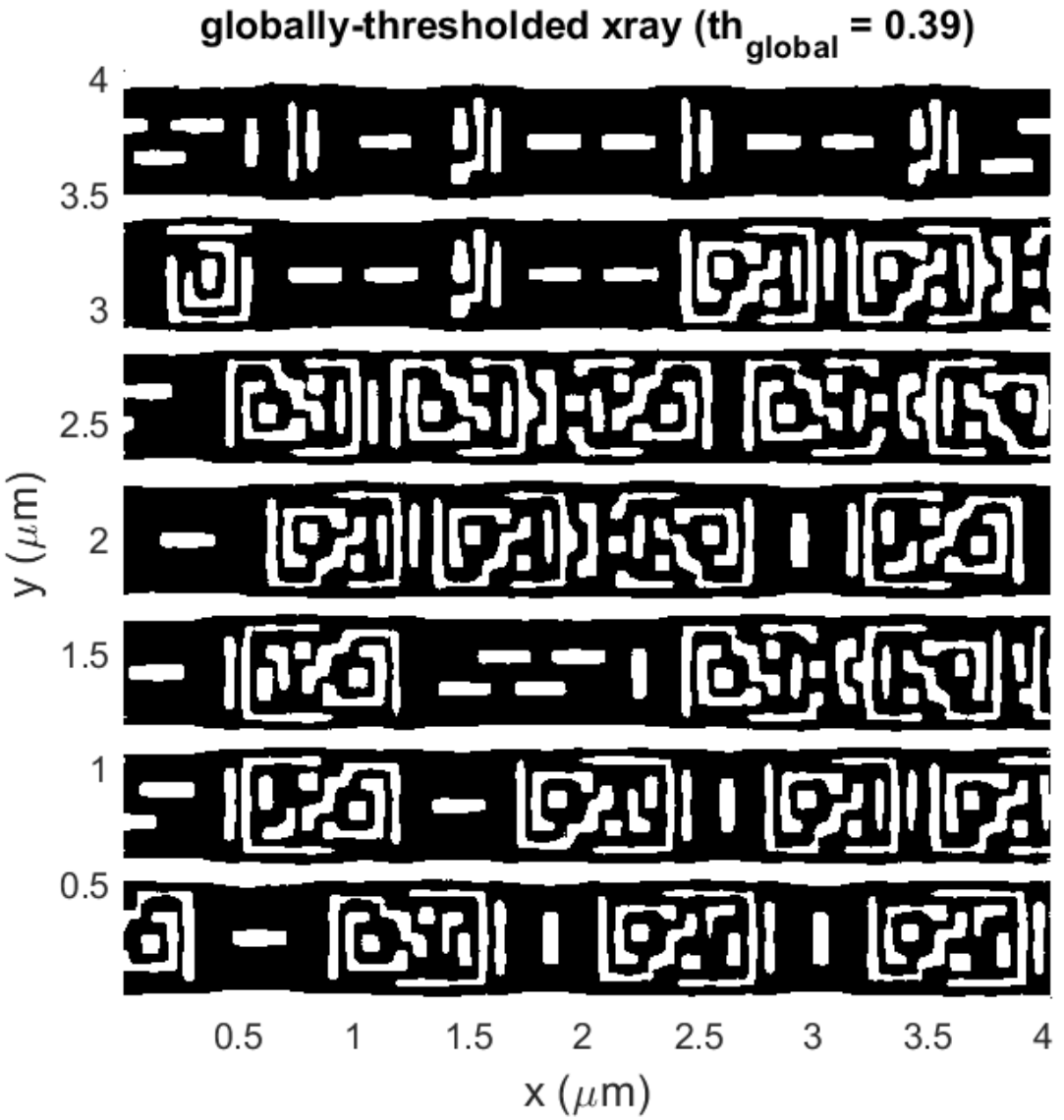




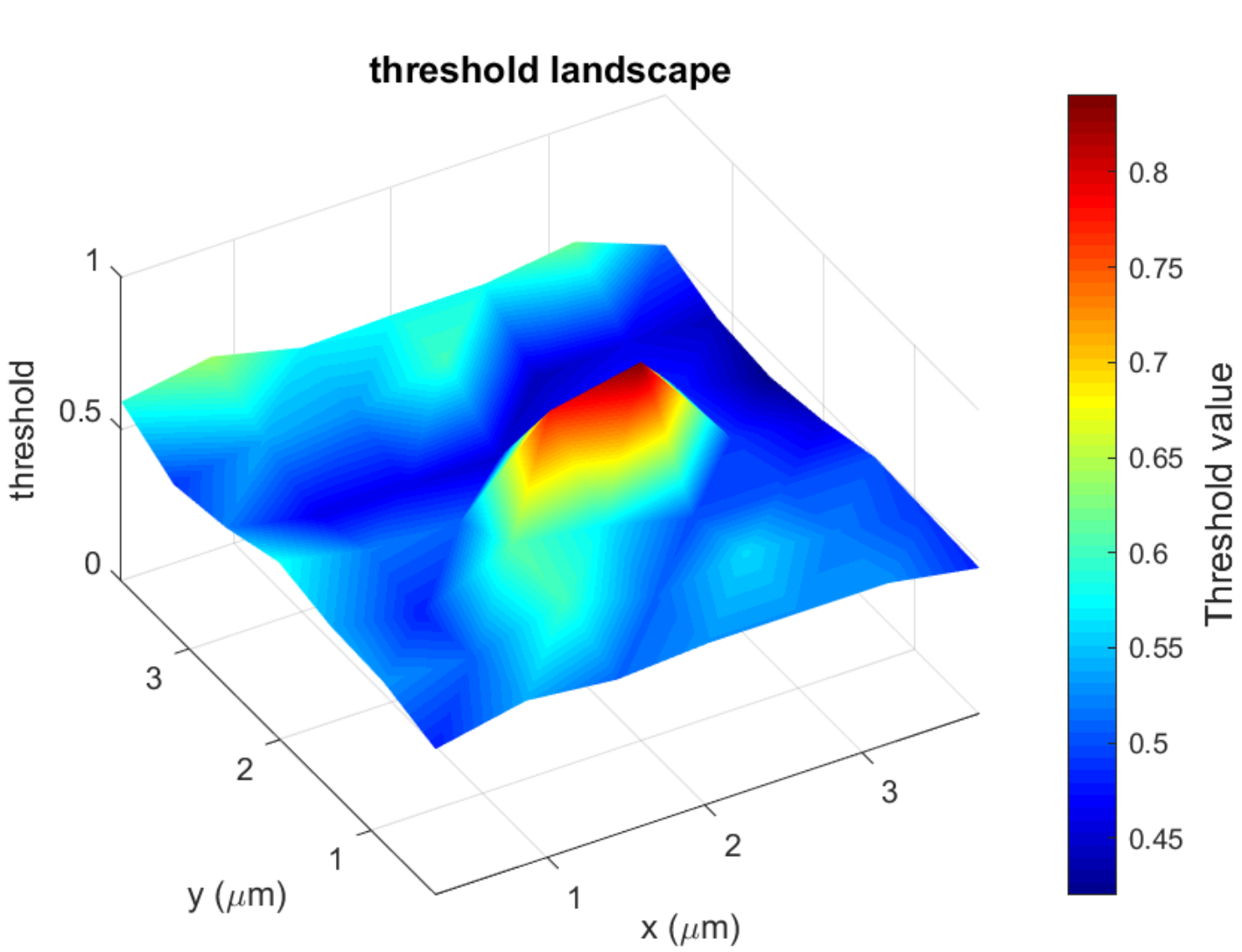

Step 1: Optimally threshold (row 1, column 1, optimal threshold = 0.66)
0.5
1
1.5
2
2.5
y (μm)
0.5
1
1.5
2
2.5
x (μm)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

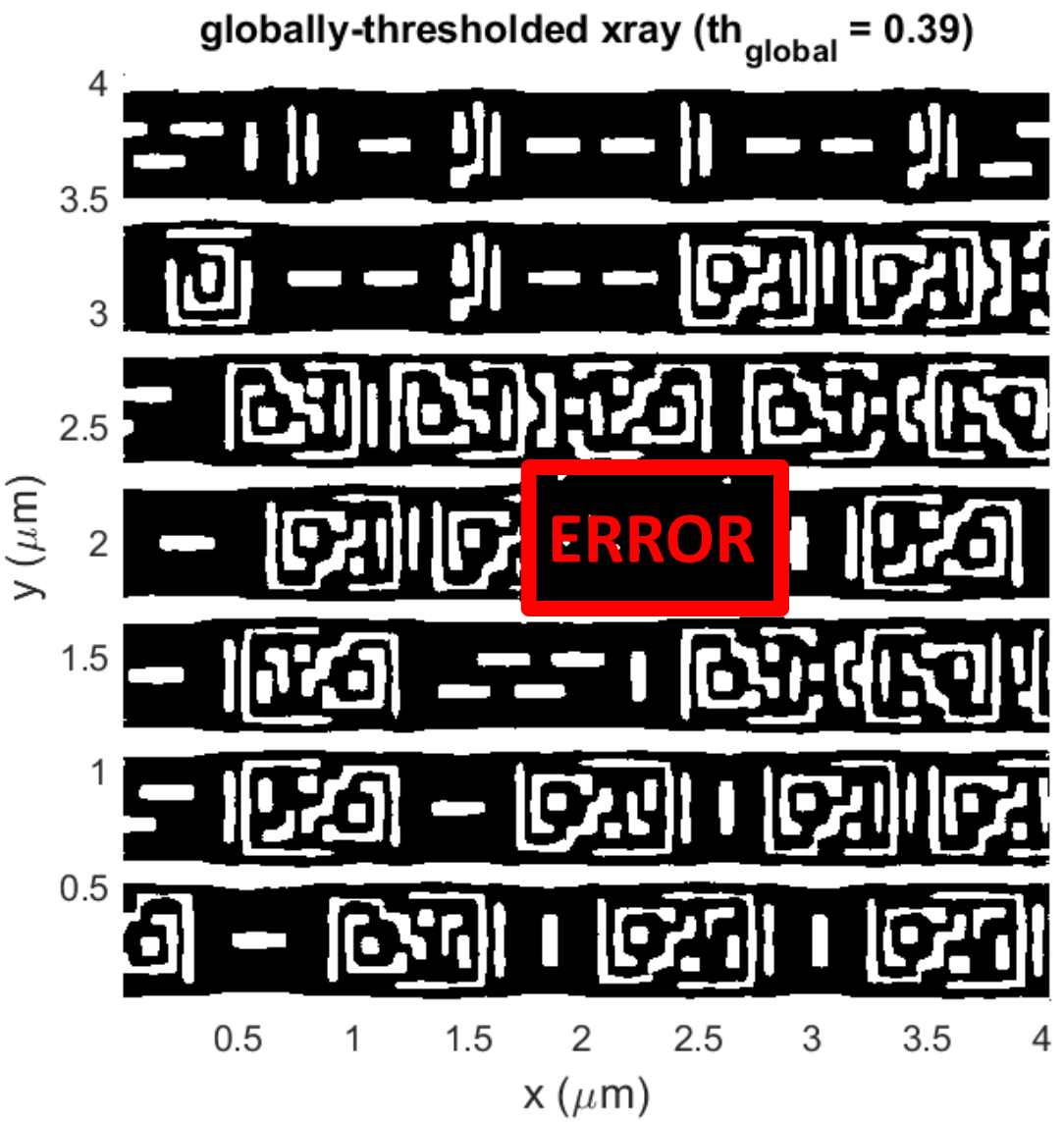
Machine-generated delayered M1 and threshold-landscape





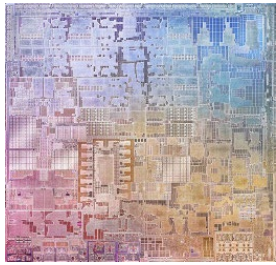
Machine-detection of error in M1 manufacture versus design



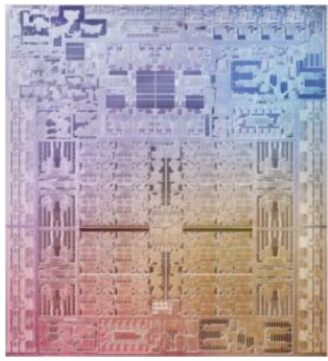


Chip Scan: 3D X-ray imaging of CMOS integrated circuits

A non-destructive 3D coherent X-ray imaging project using information-driven 3D tomography. The current state-of-the-art method is chip-scanning large-area (> 1 cm^2) CMOS integrated circuits using a coherent X-ray laminography microscope with zoom. This can be used for 3D reconstruction, virtual delayering, non-destructive automated reverse engineering, quantification of manufacturing capabilities, efficient identification of manufacturing defects, failure analysis, counterfeit products, a certified trust service, and future sub-nm resolution metrology



Contributors to the team effort: Mirko Holler, Manuel Guizar-Sicairos, Tomas Aidukas, Michal Odstrcil, Maxime Lebugle, Elisabeth Müller, Simone Finizio, Gemma Tinti, Oliver Bunk, Jörg Raabe, Gabriel Aeppli, Joshua Zusman, Walter Unglaub, Bill Taylor, Sri Samavedam, and A. F. J. Levi



Publications: M. Holler et al., *Nature Electronics* **2**, 464 (2019)

A.F.J. Levi and G. Aeppli, https://spectrum.ieee.org/chip-x-ray (2022)

I. Kang et al., *Optica* **10**, 1000 (2023)

T. Aidukas et al., *Nature* **632**, 81 (2024)

Recent progress: Since 2019, optimization of hardware and algorithms to give >100x voxel acquisition rate, 10x increase in depth of field, 4x improvement in resolution, 16x speedup using ML

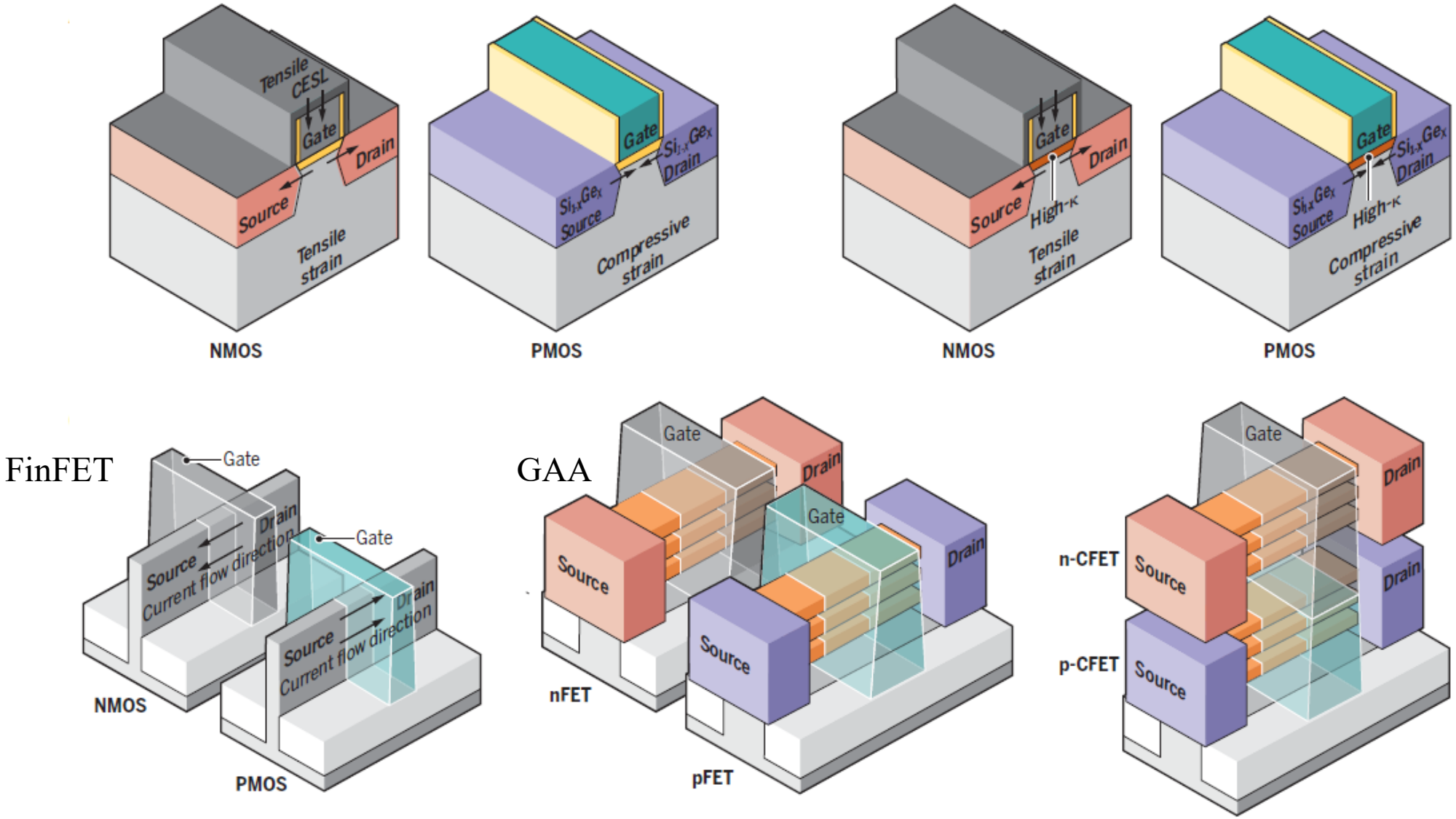
Future directions

Future technology development and demonstration

- Technology
  - 100x brilliance *after* synchrotron upgrade (4Q25)
  - 100x flux with new X-ray optics, channel-cut crystal monochromator (4Q25)
  - Installation of high count-rate “Matterhorn” detector
  - Trace materials detection with XRF (Ketek VIAMP SSD) and multimodal imaging
  - Smart Chip Scan – ML and AI

- An achievable objective
  - Near real-time 3D reconstruction of integrated circuits with sub-nm resolution

Detail of future GAA CMOS technology



Future GAA "1 nm" technology node, 500 transistors per μm^2

L_{Si} = 0.543 nm and number of atoms to model transistor and local interconnect

N_{atoms}=50×50×325×8 / L^3 = 4×10^7

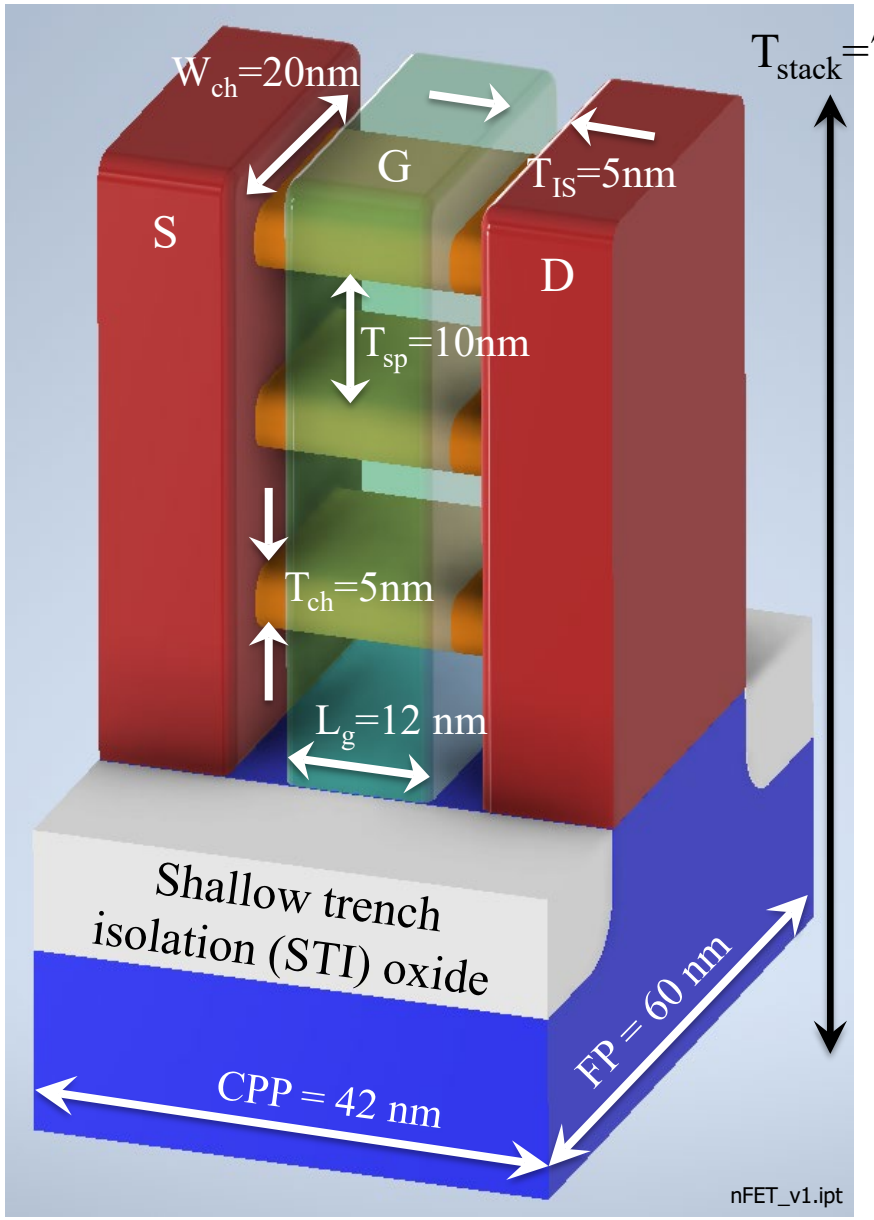
[Toward attojoule switching energy in logic transistors | Science]

Gate All-Around nanosheet FETs (GAAFETs): Conventional geometry

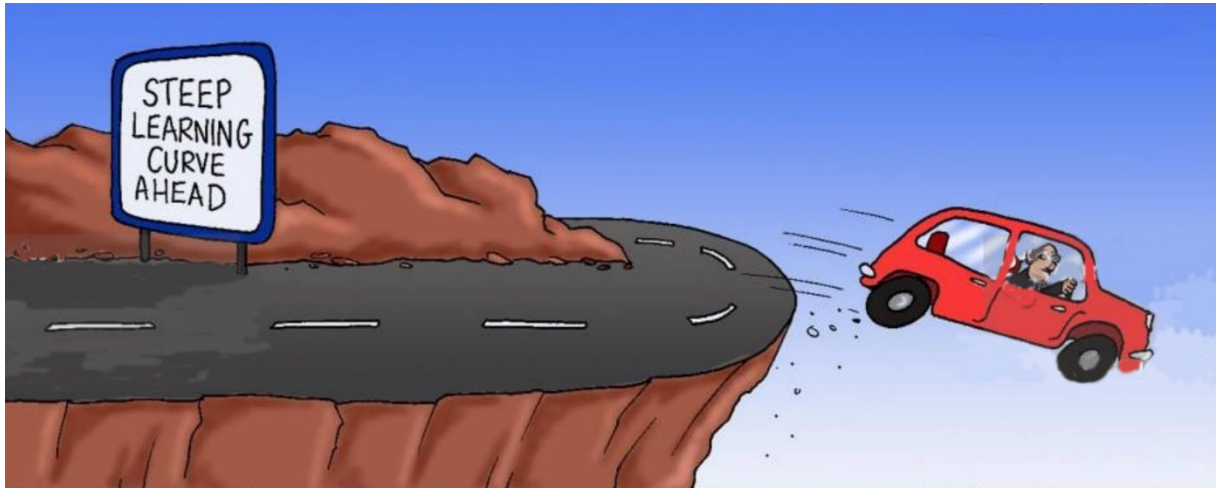
Symbol	Description	Value
CPP	Contact poly pitch	42 nm
FP	Fin pitch	60 nm
L_g	Gate length	12 nm
T_{sp}	Spacing thickness	10 nm
T_{ch}	Nanosheet thickness	5 nm
T_{IL}/T_{HK}	Interfacial layer / HfO_2	0.6 nm / 1.1 nm
T_{IS}	Inner spacer thickness	5 nm
W_{ch}	Nanosheet width	20 nm
P_{NS}	Nanosheet pitch	~16 nm
T_{stack}	Total stack thickness	~75 nm

"1 nm" technology node, L_{Si} = 0.543 nm
Number of atoms to model transistor and local interconnect
N_{atoms}=50×50×325×8 / L^3 = 4×10^7

S. Lee et al. *Nanomaterials* **13**, 868 (2023)
J. Yoon et al. *Nanowires-recent progress* (2020)



There is a lot to learn, act on, and get right …



End