Link components for a 2.5 Gb/s/channel 12-wide parallel optical interface in 0.5 μm CMOS

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Abstract: Preliminary results on a 12-wide 2.5 Gb/s/channel opto-electronic receiver array and a low jitter 0.4 - 1.6 GHz x2/x4 PLL based Frequency Synthesizer (PLLFS) in 0.5 μm CMOS technology are presented.

OCIS codes: (200.4650) Optical interconnects, (250.5980) Semiconductor optical amplifiers

Critical components needed to interface fast-narrow synchronous parallel fiber-optic interconnects to slow-wide parallel electrical interconnects are VCSEL drivers [1], a 4:1 or 2:1 multiplexer/demultiplexer array [2], a high-performance x4/x2 PLLFS and an opto-electronic receiver array. The demands of integration, cost, and compatibility with future technological improvements require that these components be in CMOS technology.

The receiver array in Fig. 1 is a latched design for a half-speed parallel optical data bus with a designated clock channel. Each front-end receiver is a common gate stage driving a Trans-Impedance Amplifier (TIA). This isolates the TIA from the PIN photo-diode capacitance and improves noise performance. The TIAs are designed to give a differential current signal from an isolated PIN.

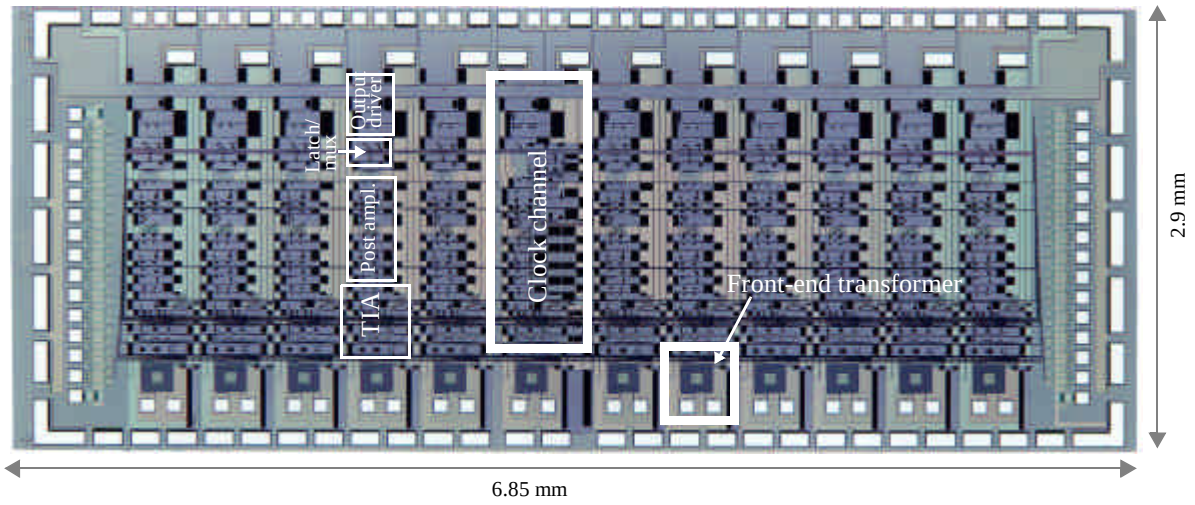

Fig. 1. Opto-electronic receiver array IC in 0.5 μm CMOS. Channels employ transformers at the front-end for noise-shaping and peaking.

A transformer implemented as coupled planar spirals on top level metal with a dedicated ground shield is used to noise shape the front-end so that a noise-minimum was achieved near 2.5 Gb/s. The post-amplifier stages implement controlled peaking to compensate for limited front-end bandwidth. Retiming the post-amplifier output effectively provides additional gain, cleans up the data eye, reduces jitter and minimizes skew.

The receiver array was tested electrically with ac-coupled differential signals and a 150 fF load capacitance. The sensitivity versus BER curves of the receiver is shown in Fig. 2 (a). Source-referenced jitter is measured to be 12.47 ps

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(rms) at -16 dBm for 2^{31}-1 NRZ PRBS (Fig. 2 (b)).

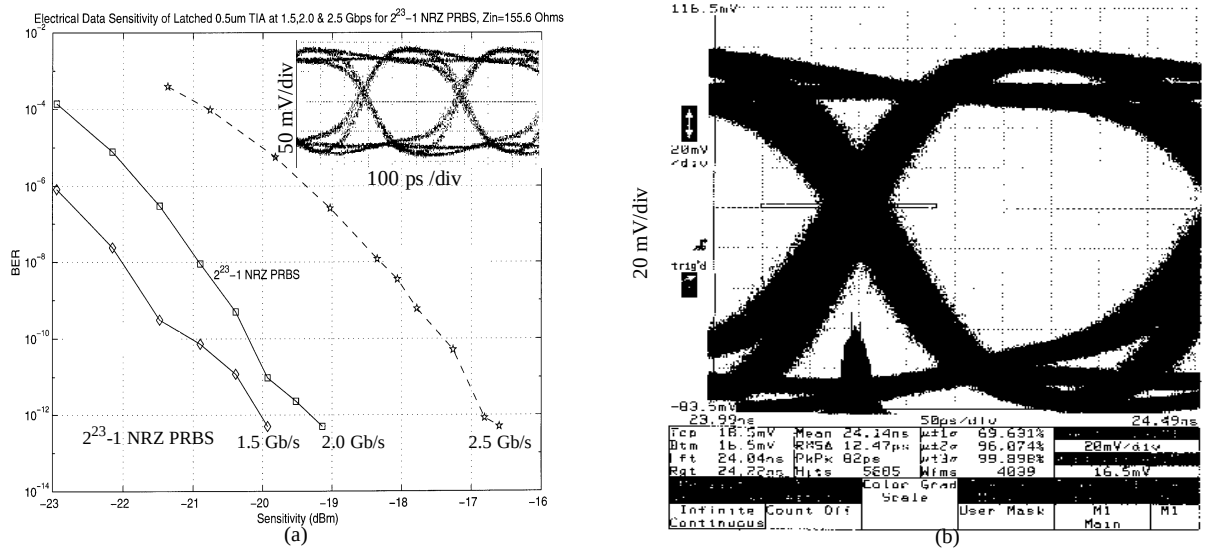

Fig. 2. (a) Measured sensitivity curves for 1.5, 2.0 and 2.5 Gb/s for 2^{23}-1 NRZ PRBS. The inset shows the output eye-diagram at 2.5 Gb/s for -16.5 dBm of input power. (b) Measured jitter of the electrical output driver of the receiver at 2.5 Gb/s for 2^{31}-1 NRZ PRBS -16 dBm data and clock. Jitter is measured to be 12.47 ps (rms) and 82 ps (pk-to-pk).

The PLLFS is characterized by a wide frequency tuning range to accomodate different system clock speeds for graceful performance degradation and ease of testing, very low jitter to minimize system insertion penalty, selectable x2/x4

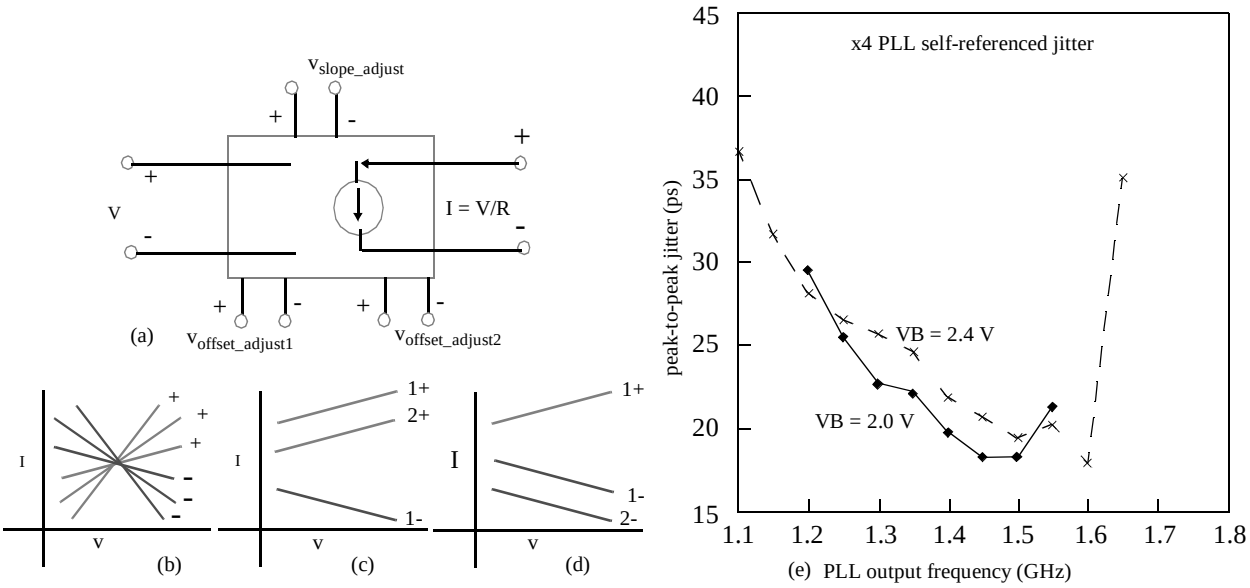

Fig. 3. (a) Schematic of the PLLFS control circuit. (b), (c) and (d) response of output I of the control circuit in (a) to the V_{slope_adjust} control, the $V_{offset\_adjust1}$ and $V_{offset\_adjust2}$ controls respectively. (e) Measured peak-to-peak jitter of the PLLFS at two oscillator settings (VB = 2.0 V and VB = 2.4 V) showing a reduction in output jitter for the x4 selection of the PLLFS. The implemented die is 3.3 mm x 1.6 mm in size.

frequency multiplication and high maximum frequency of operation for data rates in excess of 2.5 Gb/s per signal line. We use the slope and offset control of the oscillator control circuit (Fig. 3(a)) to achieve output peak-to-peak jitter of less than 25 ps at 1.25 GHz in both x2 and x4 operation. This feature of our architecture may be used to inter-

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face to a digital control circuit that puts the oscillator in a high gain setting to acquire the signal and then automatically changes the gain to reduce the jitter of the locked signal without losing lock. Fig. 3 (e) shows the measured peak-to-peak self-referenced output jitter of the x4 PLLFS demonstrating the reduction in jitter using the slope adjust control.

Preliminary measurements of the receiver give a sensitivity of approximately -20 dBm, -19 dBm and -16.6 dBm for 1.5, 2.0 and 2.5 Gb/s for 2^{23}-1 NRZ PRBS at BER < 10^{-12}. The array consumes 2.2 W *with* source terminated LVDS drivers from a 3.6 V supply. The x2/x4 PLLFS has sub-25 ps peak-to-peak jitter at 1.25 GHz and consumes 1.2 W from a 3.6 V power supply.

References:

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[2] B. Madhavan and A. F. J. Levi, '55.0 Gbps/cm data bandwidth density interface in 0.5 μm CMOS for advanced parallel optical interconnects', Electronics Letters, vol. **34**, no. 19, pp 1846-1847 (1998).

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