TE03_35 TEST AND MEASUREMENT REPORT

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Rev 0.91

1.0 TE03_35 (Second test die in 0.35 μm CMOS)

1.1 Introduction

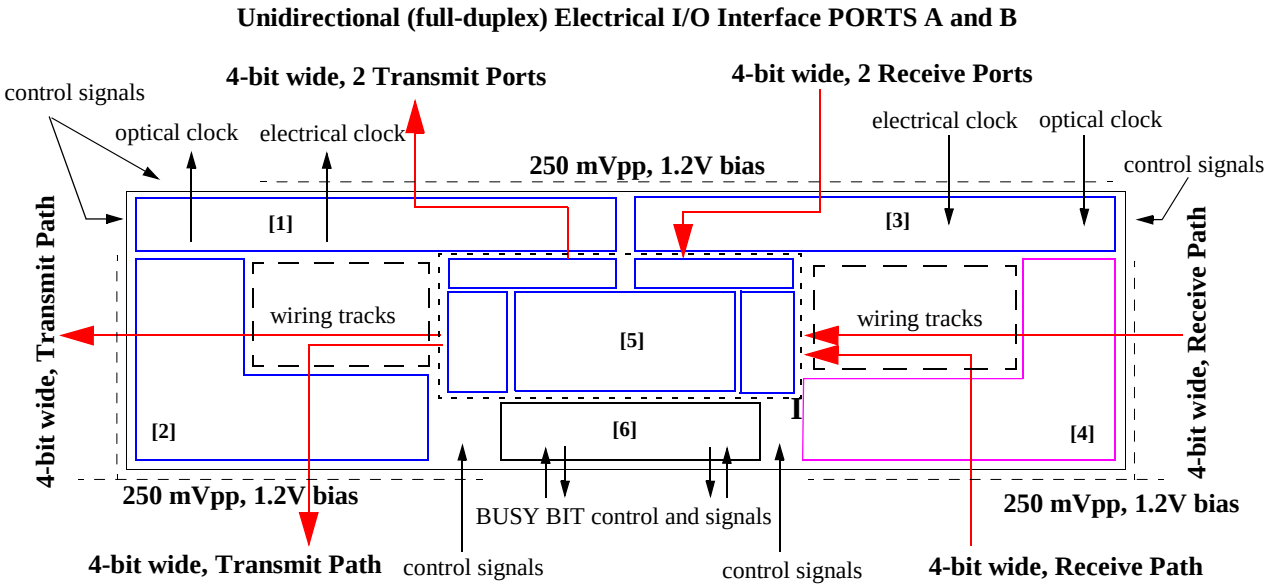
The TE03_35 Switch IC is implemented in 0.35 μm CMOS process and is similar to the original TE03 0.25 μm CMOS IC. The IC operates at 2.0 Gb/s (2.25 Gb/s best case) to fully connect 4 processors with a peak throughput of 32 Gb/s. The TE03_35 IC contains two LVDS 4-bit electrical I/O interface ports representing the electrical I/O interface of a scaled-up Switch IC. It also contains two separate LVDS 4-bit electrical input and output paths representing the optoelectronic interface of such a scaled-up IC. TE03_35 also includes BUSY BIT monitoring circuitry to monitor the processor status.

Compared to the TE02 IC, TE03_35 IC has on-chip termination for both LVDS inputs and outputs. Due to process variations the termination resistance was measured to be 88 Ohms (expected value was 45 - 60 Ohms). The common-mode voltage of the LVDS signals are assumed to be 1.2V and can also operate at 1.8V. Compared to the original TE03 0.25 μm CMOS IC, the encoded frame and busy bit LVDS outputs of TE03_35 have on-chip termination. Compared to the TE02 IC, TE03_35 boasts a 2.5 times better worst-case input sensitivity, and a 10% increased data rate.

The output LVDS drivers in TE03_35 were resized to have > 300 mVpp swing across 25 Ohms (50 ohm termination at both source and destination), and as a result the total power consumption of the IC has increased to 3.6 W (1.1 A current). The LVDS bias control voltage VTT consumes 300 mA.

The version number 1.0 will contain more test results and testing information.

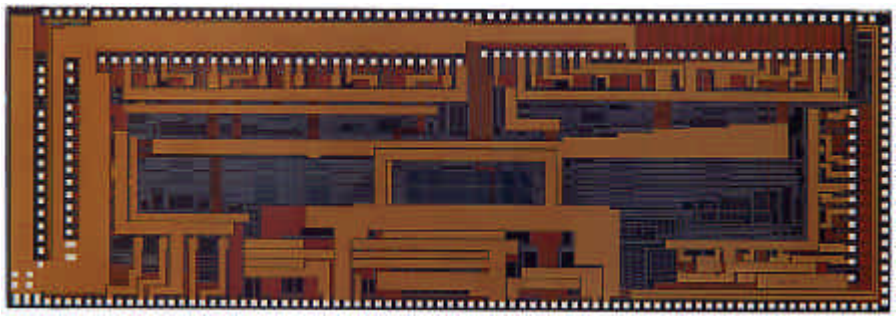
Layout organization:



1. 4-bit wide, 2 Port transmit circuitry (electrical output interface)
2. 4-bit wide, 2 Path transmit circuitry (represents the optical output interface)
3. 4-bit wide, 2 Port receive circuitry (electrical input interface)
4. 4-bit wide, 2 Path receive circuitry (represents optical input interface)
5. Switch core
6. BUSY BIT circuitry

Switch internal clock domain
Optical clock domain
Synchronization boundary clock domains
Data flow

FIGURE 1: Layout organization of TE02 showing the major blocks (9.0 mm x 2.2mm)



Ship date: 06/12/2000
Return date: 07/21/2000
Process: 0.35 µm CMOS
Size 9.0 x 3.0 mm^2

1.2 IC Functionality

Data path:

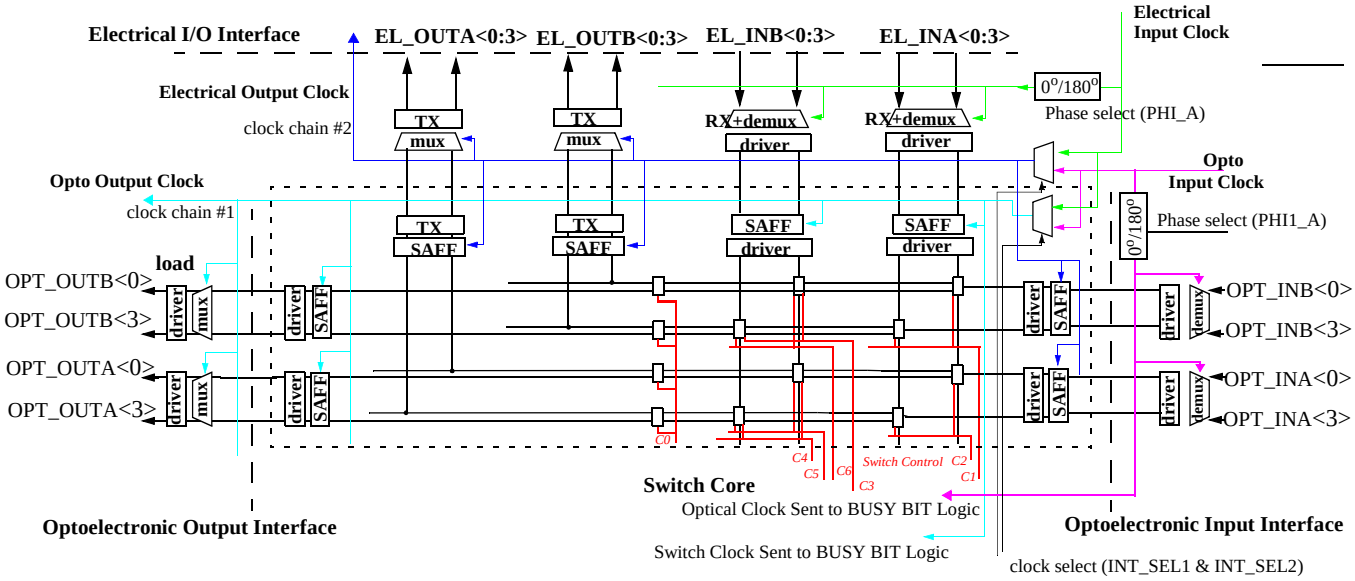


FIGURE 2: Abstract of the TE03 IC, without BUSY BIT monitoring circuitry

Figure 2 shows an abstract block diagram of the data path. PORT A (EL_INA,EL_OUTA) and PORT B (EL_INB, EL_OUTB) are the electrical I/O interface. OPT_INA and OPT_INB represent the optoelectronic inputs, while OPT_OUTA and OPT_OUTB represent the optoelectronic outputs. Note that the high-speed inputs to the IC are on the right and the high-speed outputs are on the left.

Input data are demuxed by 2 at the input, and are muxed again at the output. A half-speed clock is used for receiving and transmitting the data. The IC has two clock domains, and two possible clock inputs, both of which are received electrically at the right top of the IC. One clock is the electrical input clock, and the other is the mock optical clock which represents the optoelectronic input clock.

The switch core contains SAFFs and drivers at its boundary (Figure 2), and the internal switching is implemented using pass-transistor logic. Though a 4x4 full crossbar switch requires 2^4 (16) control lines, since the te03_35 switch IC is designed for a FRP network, only 7 control lines are provided. Since the switch was designed based on the earlier te02 IC, there is a certain

amount of redundancy in the control lines. As a result of the reduced number of control lines compared to a full crossbar switch the following input/output mappings are not allowed.

OP_INB → OP_OUTA
OP_INA → OP_OUTB
OP_INB → EL_OUTA
OP_INA → EL_OUTB

These mapping were not included in the switch configuration as they are not required for FRP network. A program "crossconnect" (written in C) is available and can be used to find all input/output mappings, input/output mappings corresponding to a particular control input combination, or to find the required control input combination for a particular input/ output mapping.

Some important switch configurations are shown in Figure 3.

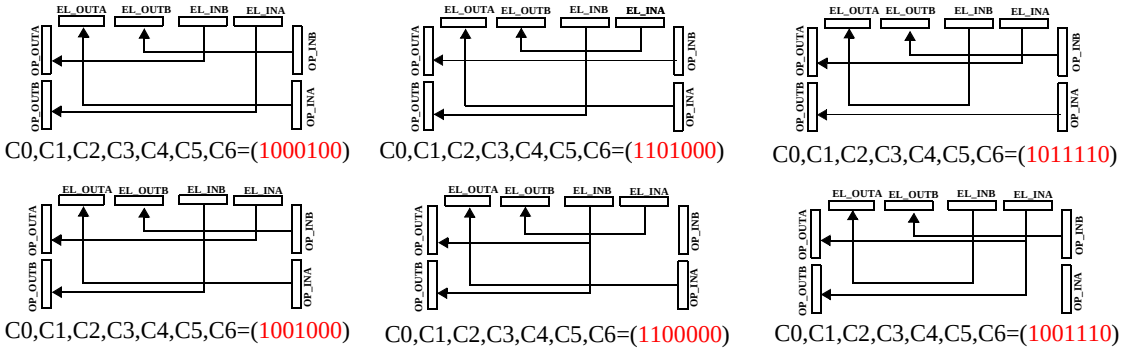


FIGURE 3: Some interesting switch configurations

Clocking:

In Figure 2, the two clock domains have different colors. The switch internal clock is blue, while the mock optical clock is magenta and mock electrical clock is light green. Both clocks are received using LVDS receivers, and go through a delay chain. The signals SEL_ELEC and SEL_OPT are provided to bypass the delay chain. The level shifting of the clock is done after the delay chain, and before the delay chain bypass mux. The signals INT_SEL1 and INT_SEL2 specify which clock is used as the switch internal clock.

A $0^o/180^o$ degree phase selection circuit is used at both the electrical and mock optical interfaces to control the relative phase of the electrical and optical interface clocks to the switch internal clock. The signal phase select PHI_A and PHI1_A controls the $0^o/180^o$ phase selection circuits.

Two analog signals, BIAS_CONTE and BIAS_CONTO are provided to control the duty cycle of the mock optical and electrical clocks.

In the Switch IC there are no feedback loops between stages, and data has a right-to-left flow. This data flow pattern is used to simplify the IC clock routing.

Even though the BUSY BIT logic can be designed to have its own separate clock, even in TE03_35, the BUSY BIT logic shares the same mock optical and switch internal clocks with the data path.

BUSY BIT Circuit

In addition to the data path, the TE03_35 also implements a BUSY BIT scheme for network access arbitration. The BUSY BIT provides information about the status of the processors in the network. A high value indicates that a processor is busy, while a low value indicates that it is available. If individual processors in network do not share the paths and BUSY BITs, then a network with *N* processors (optical paths), requires *N* BUSY BITs for network access arbitration.

The BUSY BITs can be implemented using a dedicated optical channel per BUSY BIT (a dedicated TOKEN per processor), or by serializing the BUSY BIT information on one optical channel. In the case of a dedicated TOKEN, an active low TOKEN pulse circulating in the network indicates that a processor is free. A processor P_j can grab a free processor P_i, if the TOKEN pulse corresponding to P_i is currently at P_j's Switch IC. P_j grabs the free TOKEN by inhibiting the propagation of the pulse. In this case the pulse itself indicates the time frame at which the TOKEN can be grabbed. Thus, there is no need for an additional FRAME bit. Note that a static low voltage cannot be used to indicate a processor is free, since more than one processor may grab it simultaneously.

On the other hand, when the BUSY BIT information is serialized into one or more optical channels, there is a stream of 1's and 0's (stream of pulses) flowing in the network. In this stream of information, we need to know exactly where BUSY BIT *i* is located. Thus, there needs to be scheme to identify the starting and ending point of the data stream. An additional FRAME signal is used for this purpose.

The FRAME constantly circulates around the network on its own dedicated optical channel. Another dedicated optical channel caries the processor BUSY BITs, which are encoded serially starting with the BUSY BIT for processor *n*, at the 0→1 transition of the FRAME. The total FRAME/BUSY BIT latency is 4 cycles:

- 2 cycle latency due to FRAME receiving and buffering
- 2 cycle latency due to decoding/encoding required for AC coupling.

Figure 4 shows an abstract block diagram of the BUSY BIT circuit. It consists of a request interface register, a request register, a grab register, and a grab interface register. The request interface register is the external interface to the request register. The request register holds which processor BUSY BITs are being requested by this node. The grab register saves which BUSY BITs have been obtained by this node, and the grab interface register is the external interface to the grab register.

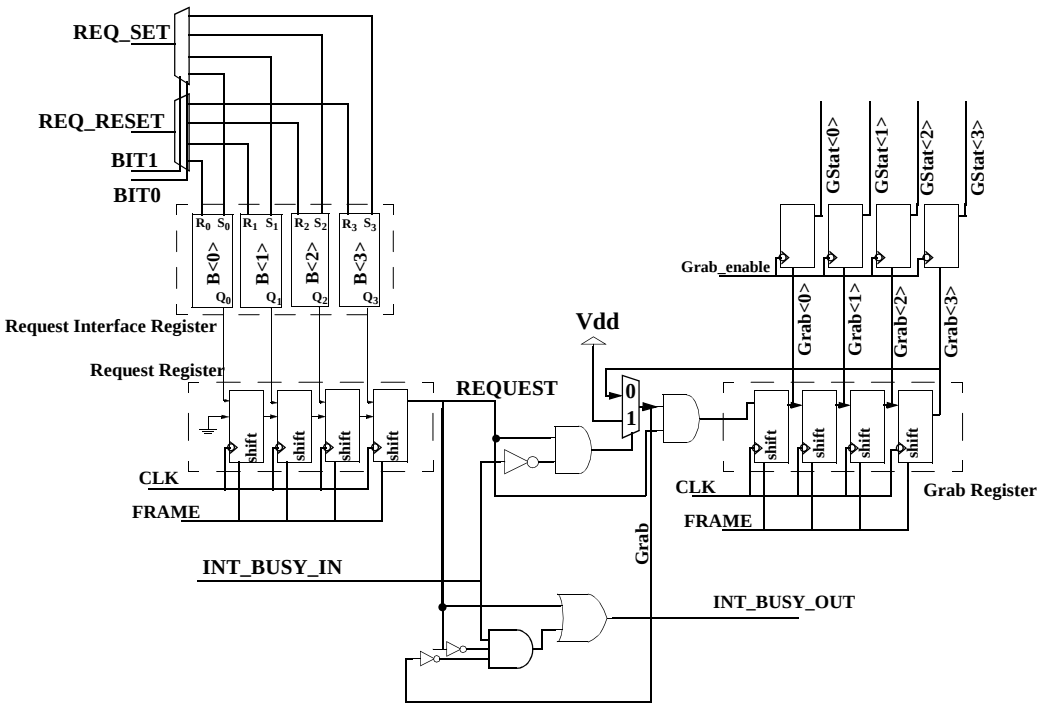


FIGURE 4: Abstract of the BUSY BIT monitoring circuitry

Request interface register:
The request interface register is the interface between the request register and the external world. It consists of RS latch type FFs, and is controlled by external inputs BIT<1:0>, REQ_SET (REQSET2) and REQ_RESET (REQRESET2). The bits BIT<1:0> specify the appropriate request interface register, and REQ_SET specifies a set operation while REQ_RESET specifies a reset operation. BIT1 and BIT0 must remain stable when REQ_SET or REQ_RESET is active. The truth table for the request control interface is given in Table 1.

Request register:
The request register holds which processor BUSY BITs are being requested by this node, and consists of sense-amp FFs which load at the falling clock edge. When FRAME is low (inactive FRAME), the request interface register values are continuously loaded into the request register. During FRAME the values stored in the request register are right-shifted. During this right-shift, the left most bit of the request register loads a low value. In addition to handing BUSY BIT requests during normal operation, the request register is also used by the master node to set the length of the FRAME during FRAME creation.

Grab register:
The grab register saves which BUSY BITs have been obtained by this node. During FRAME low, the grab register retains its values. During FRAME, the grab register is right-shifted, with the input at the left-most SAFF being a function of the current output of the right-most SAFF, the input BUSY BIT value, and the REQUEST signal:
GRAB = REQUEST.$\overline{(BUSY\_IN}$ + GRAB<3>)

Grab interface register:
The grab interface register is the interface between the grab register and the external world. When the input grab_enable is active (set to low), the grab register values are loaded into the grab interface register. Grab_enable should only be activated when the FRAME is not present at the node, preferably right after a FRAME has past the node. Grab interface register signal GSTAT<3:0> show which processor BUSY BITs were grabbed by this node.

The LVDS (unterminated) outputs LVDS_TOm and LVDS_TOp can be used to monitor the received FRAME as well as to load the grab interface registers. A 0→1 transition on the grab interface register clock (clkock_in2) will load the grab interface registers. The output LVDS_TOPp (polarity inverted relative to the internal FRAME) can be used as the grab interface register clock (clkock_in2). A resistance of > 150 Ohms to ground can be connected at the LVDS_TOPp output to generate a 2.0V swing to be used as the grab interface clock. Since LVDS_TOp and LVDS_TOm are unterminated, an external termination of 50 Ohms to VTT can be connected to LVDS_TOm to monitor the internal FRAME signal.

Table 1: Truth table for the request interface register

REQSET2	REQRESET2	BIT1	BIT0	Reset				Set				Request interface register output
				R_3	R_2	R_1	R_0	S_3	S_2	S_1	S_0	
0	0	X	X	0	0	0	0	0	0	0	0	Inactive set/reset
1	0	0	0	0	0	0	1	0	0	0	0	reset #0, $Q_0 = 0$
1	0	0	1	0	0	1	0	0	0	0	0	reset #1, $Q_1 = 0$
1	0	1	0	0	1	0	0	0	0	0	0	reset #2, $Q_2 = 0$
1	0	1	1	1	0	0	0	0	0	0	0	reset #3, $Q_3 = 0$
0	1	0	0	0	0	0	0	0	0	0	1	set #0, $Q_0 = 1$
0	1	0	1	0	0	0	0	0	0	1	0	set #1, $Q_1 = 1$
0	1	1	0	0	0	0	0	0	1	0	0	set #2, $Q_2 = 1$
0	1	1	1	0	0	0	0	1	0	0	0	set #3, $Q_3 = 1$
1	1	X	X	-	-	-	-	-	-	-	-	Not allowed

Figure 5 shows an abstract timing diagram of a processor REQUEST and GRAB operation. First the requesting processor sets the request interface register bit corresponding to the desired processor BUSY BIT (when FRAME is not present). If the corresponding BUSY BIT is free, when FRAME arrives the node sets the BUSY BIT and record the fact that it grabbed the bit in the grab register. To read the Grab Register, the processor activates the grab_enable signal, which loads the grab register values into the grab interface register (when FRAME is not present).

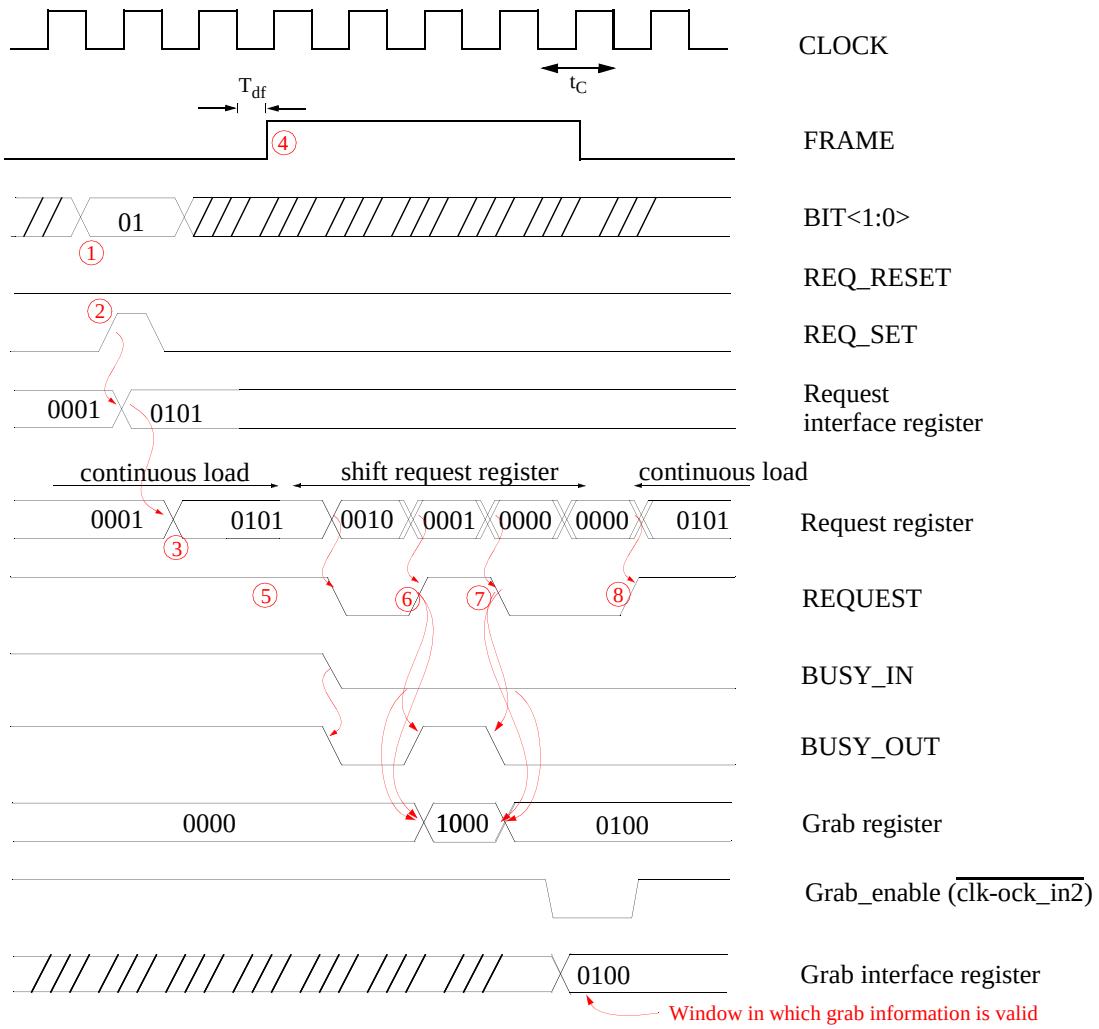


FIGURE 5: Abstract timing diagram showing the request and grabbing of BUSY BIT for P_1

The following steps trace the operation of the external control and internal signals for the case of requesting the BUSY BITs for processors P_1 and P_3 and successfully grabbing the BUSY BIT for P_1.

Step #1
Select the request interface register bit corresponding to the BUSY BIT being requested or released, in this case the BUSY BIT for P_1. BIT<1:0> = 01 decodes to BUSY BIT #1. Note that in this example both the request interface and request registers already have the bit for processor P_3 set.

Step #2
Activate the SET signal. This sets the #1 bit of the request interface register (bits are numbered from #0-#3).

Step #3.
Since FRAME is not present, at the negative edge of the clock, the new value of request interface register is loaded to the Request Register.

Step #4
FRAME arrives at the node and starts the shifting of both the request and grab registers.

Step #5
Though REQUEST (for P_3) is high, since BUSY_IN is high indicating that P_3 is already busy, the node is unable to grab P_3. Therefore a zero is be shifted in to the grab register indicating that P_3 was not grabbed, and BUSY_OUT is high.

Step #6
Since REQUEST (for P_1) is high and BUSY_IN is low indicating P_1 is free, the node is able to grab the BUSY BIT for P_1. Thus, a '1' (high) is shifted into the grab register, and BUSY_OUT is high.

Step #7
Since REQUEST (for P_0) is low, indicating that the node is not requesting P_0, and since BUSY_IN is low, indicating P_0 is free, BUSY_OUT is low.

Step #8
FRAME has left the node, ending the shifting of the request and grab registers. Therefore the request register returns to continuously loading of the request interface register.

$$\text{FRAME\_OUT} = \text{FRAME}$$
$$\text{FRAME} = \overline{\text{MS}}.\text{FRAME\_IN} + \text{MS}.\overline{\text{FC\_IN}}.(\text{HIF.REQUEST} + \overline{\text{HIF}}.\text{FRAME\_IN})$$
$$\text{HIF} = \text{MS}.(\text{FC\_IN} + \text{HIF.REQUEST})$$

FIGURE 6: Logic equations of the FRAME circuit

Figure 6 shows both the FRAME and HIF (Hide Incoming Frame) logic. The FRAME circuit is used to create and to receive the FRAME. TE03_35 uses a static chip input MS+ to identify which processor node is the master and can therefore create a new FRAME. An additional chip input (FC_IN) tells the master's Switch IC when to create a new FRAME. The FRAME logic has three possible states:

1. FRAME initialization (Can only be done by the master, and sets the outgoing FRAME to low, regardless of the incoming FRAME). When both MS (MTm = 0) and FC_IN (TCp = 1) are high, the internal signal HIF is activated (is high).
2. FRAME creation (Can only be done by the master, and creates the FRAME, only after the FRAME has been properly initialized before this stage is entered). During FRAME creation, the signal HIF is active and FRAME_OUT = FRAME = REQUEST. REQUEST is the output of the request register, which right-shifts during FRAME creation. The length of the FRAME is determined by the number of 1's in the request register. If there are *m* number of 1's in the request register (right to left), then the length of the FRAME is *m+1*. When REQUEST finally goes low, the FRAME and HIF go low completing the FRAME creation.
3. FRAME pass-through (All processor nodes except the master are always in this state, and after FRAME creation, the master node goes to this state). During pass-through the internal signal HIF is inactive (low).

Note that when FRAME is first created, the master grabs all the BUSY BITs except its own. The master then subsequently releases the BUSY BITs. This scheme allows the master to communicate with each of the nodes of the network during initialization.

State diagram in Figure 7 illustrates the three possible states of the FRAME logic.

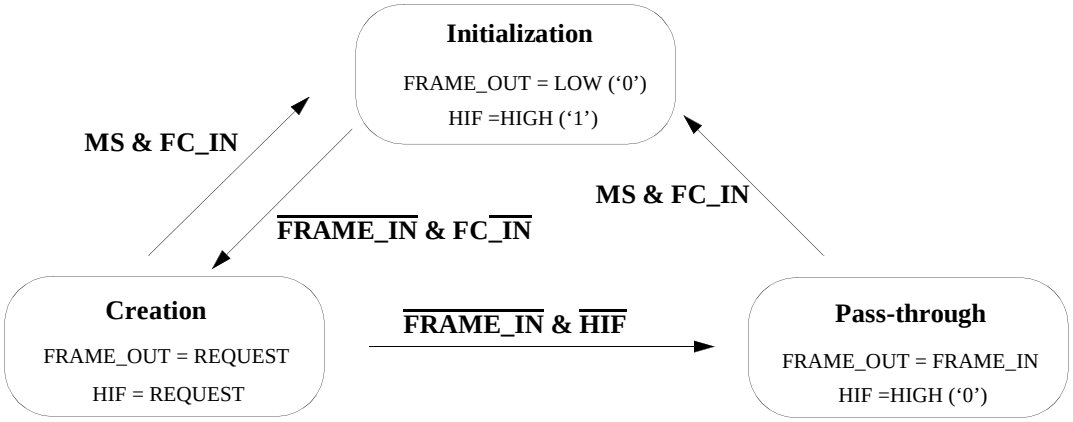


FIGURE 7: State diagram of the FRAME logic

Figure 8 shows an abstract timing diagram of the FRAME creation process. When MS and FC_IN are both active, FRAME_OUT goes low. FC_IN should only be released after enough time has elapsed for the FRAME to circulate around the network and arrive at the master node.

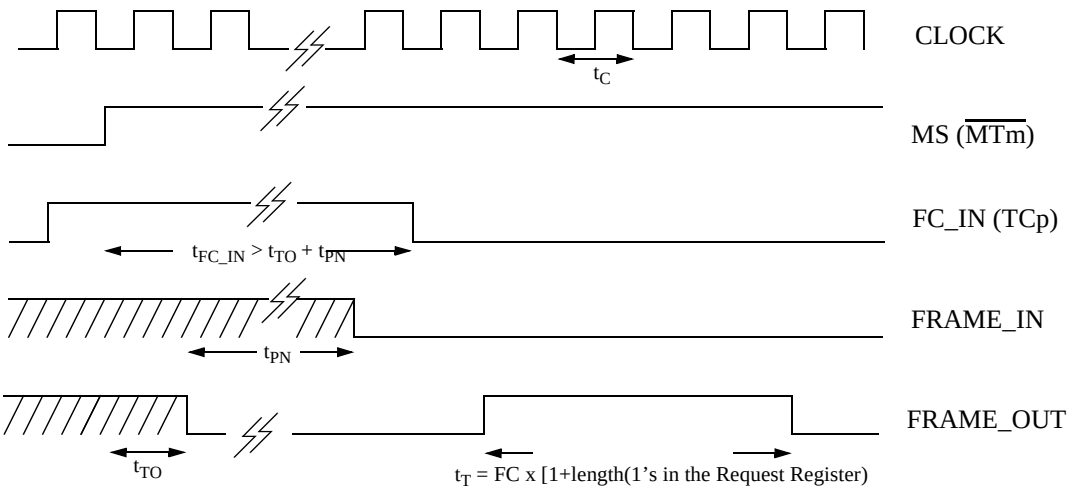


FIGURE 8: Abstract timing diagram of the FRAME creation operation

Additional characteristics of the BUSY BIT operation are as follows:

1. The request interface register, the request register, and the grab register are *n* bits wide, where *n* is the maximum number of processors that can be monitored by the IC. (4 in the case of TE03_35).
2. If the input BUSY BIT corresponding to a particular processor that we are requesting is reset (processor available), then the outgoing BUSY BIT and the corresponding GRAB bit is set.
3. If the incoming BUSY BIT corresponding to a particular processor that we are requesting is already set (processor busy), the outgoing BUSY BIT remains high, but the corresponding GRAB bit won't be set.
4. On the other hand, in case #3, if we had previously grabbed the BUSY BIT (so the grab register bit corresponding to it is set), and if we are no longer requesting that bit, then the outgoing BUSY BIT and the corresponding grab register bit is reset.

This BUSY BIT scheme can also support a two-way communication protocol (such as request/reply), in which whenever processor P_i connects to P_j, P_j connects to P_i.

To create such a connection pattern, the protocol can allow P_i to grab both P_i's and P_j's BUSY BITs. In this case there are cyclic

dependencies, and as a result network is not deadlock free. To recover from deadlock, one can implement a time-out strategy. The impact of a time-out scheme on the latency and throughput of the network is proportional to the network's deadlock probability.
The above deadlock condition can be avoided by requiring the P_j (the reply node) grab the BUSY BIT for P_i (the request node) to complete the communication. In this case the reply latency dependents on the number of processors that are trying to communicate with P_i. Here the worse case latency is equal to the total number of processors times the transmission time of a data packet.
To over come this problem, the proposed BUSY BIT scheme can be extended to limit the worse case reply latency to the transmission time of a data packet.

We have adopted a simple encoding to support AC coupling of the BUSY BIT and FRAME signals. An internal signal of "1" (HIGH) is encoded as "10", and an internal signal "0" is encoded as "01". As seen in Figure 9, this encoding strategy switches at the data rate of the IC, except during a transition.

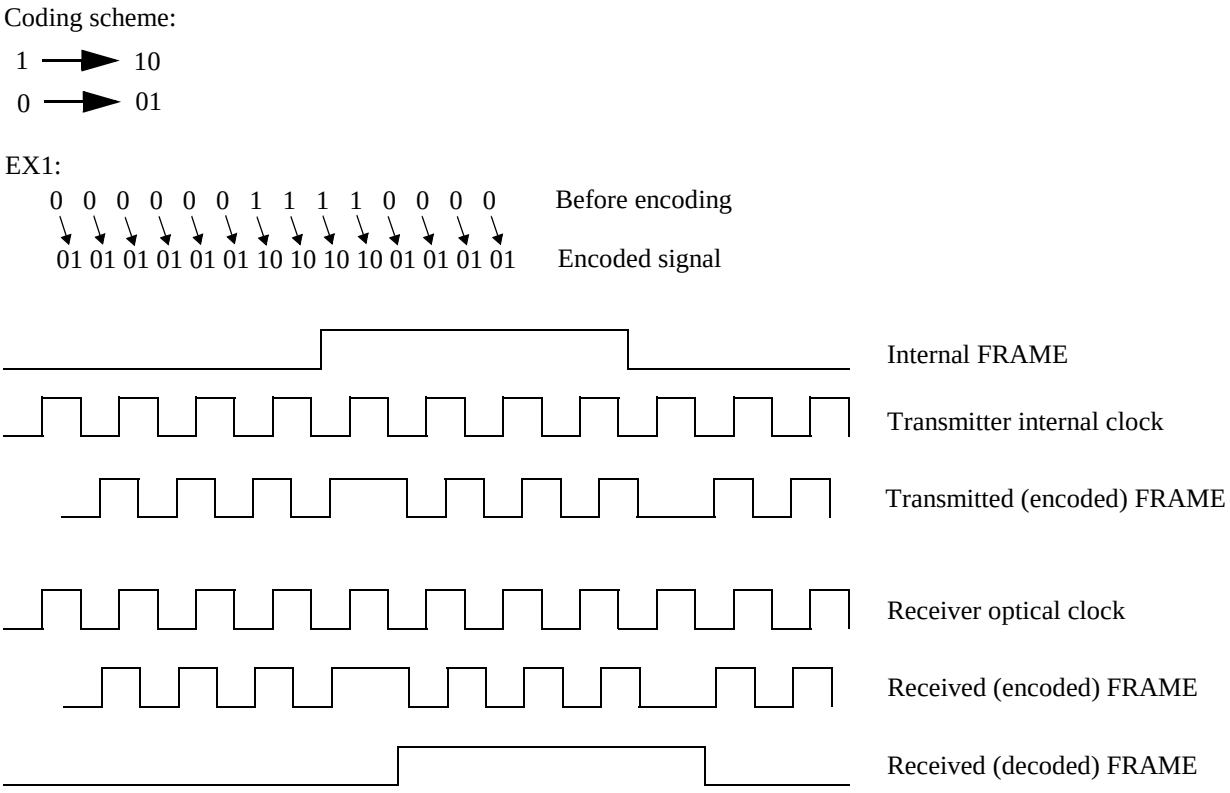


FIGURE 9: Encoding strategy employed for BUSY BIT and FRAME

1.3 Power consumption of TE03_35

The TE03_35 Switch IC is partitioned into 6 major blocks (Electrical receive, optical receive, switch core, electrical transmit, optical transmit and BUSY BIT circuitry). Simulation results show that the SA-Demux circuit consumes 11mW, and the latch and driver circuits together consume 13 mW of power. The measured power consumption of the IC is 3.6 Watts. Package and pad description

1.4 Ceramic package and cavity

Figure 10 shows the chip package, and the pin-out of the IC is shown in Table 2. It also shows the correspondence between the pad names, package pins, and the test board pin names.

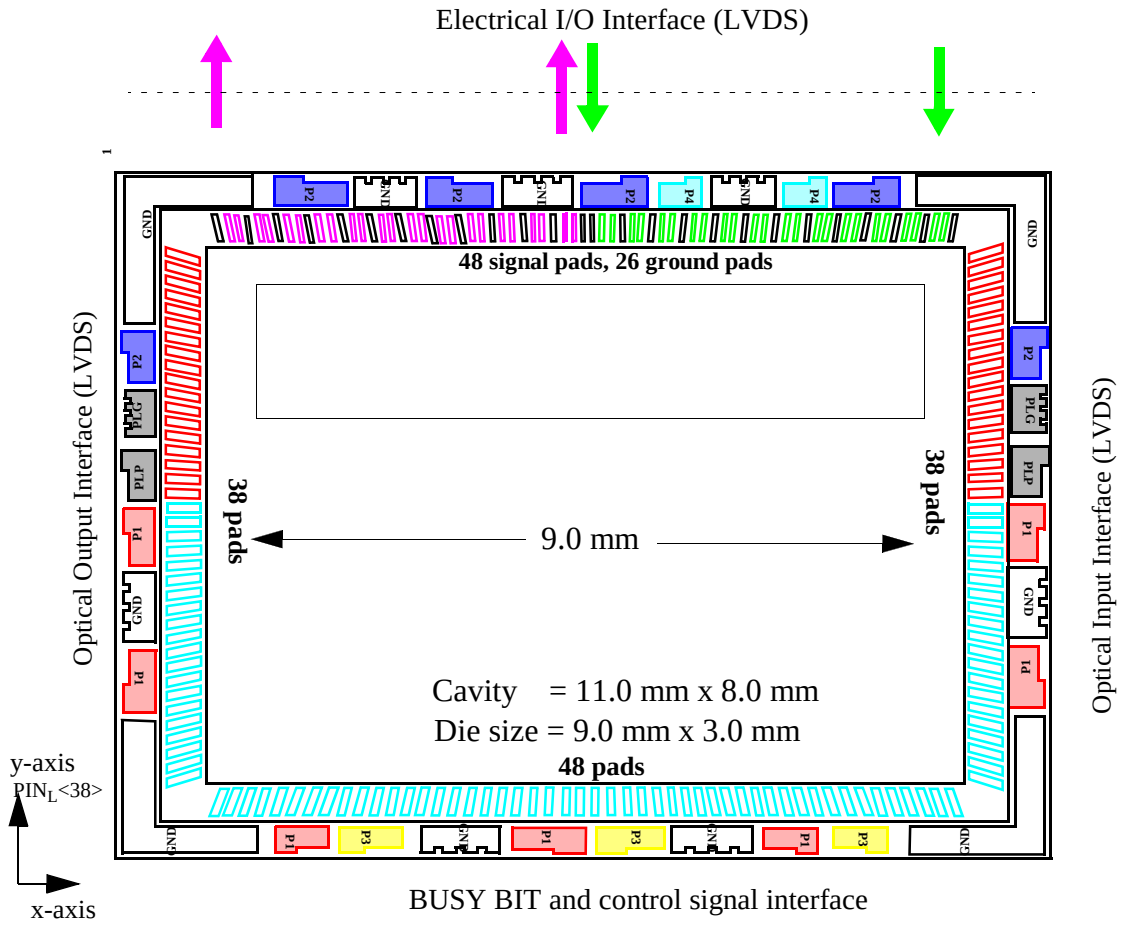


FIGURE 10: Ceramic package and cavity

Pad description

Table 2: Pin-out for TE03_35

Inputs:	*Package pin*	*Test board pin*	***Reff to VTT***	***Input / Output***	***Type***	***Swing***	***Common mode***
Clock inputs:							
lvds_oclkp	238	PDIN5+	50	Input	LVDS	250.0 mV	1.2 V
lvds_oclkm	237	PDIN5-	50	Input	LVDS	250.0 mV	1.2 V
lvds_eclkp	231	PCLK_IN_+	50	Input	LVDS	250.0 mV	1.2 V
lvds_eclkm	230	PCLK_IN_-	50	Input	LVDS	250.0 mV	1.2 V
Data inputs: (has on chip destination termination)							
lvds_a1p	236	PDIN4+	50	Input	LVDS	250.0 mV	1.2 V
lvds_a1m	235	PDIN4-	50	Input	LVDS	250.0 mV	1.2 V
lvds_a2p	233	PDIN3+	50	Input	LVDS	250.0 mV	1.2 V
lvds_a2m	232	PDIN3-	50	Input	LVDS	250.0 mV	1.2 V
lvds_a3p	228	PDIN2+	50	Input	LVDS	250.0 mV	1.2 V
lvds_a3m	227	PDIN2-	50	Input	LVDS	250.0 mV	1.2 V
lvds_a4p	226	PDIN1+	50	Input	LVDS	250.0 mV	1.2 V
lvds_a4m	225	PDIN1-	50	Input	LVDS	250.0 mV	1.2 V
lvds_b1p	223	PDIN0+	50	Input	LVDS	250.0 mV	1.2 V
lvds_b1m	222	PDIN0-	50	Input	LVDS	250.0 mV	1.2 V
lvds_b2p	221	PCIN1+	50	Input	LVDS	250.0 mV	1.2 V
lvds_b2m	220	PCIN1-	50	Input	LVDS	250.0 mV	1.2 V
lvds_b3p	218	PCIN0+	50	Input	LVDS	250.0 mV	1.2 V
lvds_b3m	217	PCIN0-	50	Input	LVDS	250.0 mV	1.2 V
lvds_b4p	216	PFRIN+	50	Input	LVDS	250.0 mV	1.2 V
lvds_b4m	215	PFRIN-	50	Input	LVDS	250.0 mV	1.2 V
Outputs:							
Clock outputs: (has on chip source termination)							
	190	PDOUT5+	50	Input	LVDS	250.0 mV	1.2 V
lvds_ooclkm	191	PDOUT5-	50	Input	LVDS	250.0 mV	1.2 V
lvds_oeclkm	197	PCLK_OUT_+	50	Input	LVDS	250.0 mV	1.2 V
lvds_oeclkp	198	PCLK_OUT_-	50	Input	LVDS	250.0 mV	1.2 V
Data outputs: (has on chip source termination)							
lvds_ob4m	192	PDOUT4+	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob4p	193	PDOUT4-	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob3m	195	PDOUT3+	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob3p	196	PDOUT3-	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob2m	200	PDOUT2+	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob2p	201	PDOUT2-	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob1m	202	PDOUT1+	50	Output	LVDS	250.0 mV	1.2 V
lvds_ob1p	203	PDOUT1-	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa4m	205	PDOUT0+	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa4p	206	PDOUT0-	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa3m	207	PCOUT1+	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa3p	208	PCOUT1-	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa2m	210	PCOUT0+	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa2p	211	PCOUT0-	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa1p	212	PFROUT+	50	Output	LVDS	250.0 mV	1.2 V
lvds_oa1m	213	PFROUT-	50	Output	LVDS	250.0 mV	1.2 V

Optical side:

			Reff to VTT	*Reff to VDD*	*Reff to GND*	*Diode forward turn on (VDD)*	*Diode forward turn on (GND)*
Inputs:	*Package pin*	*Test board pin*					
Data inputs: (has on chip destination termination)							
sig_oa4m	16	HSCTRL7	50	Input	LVDS	250.0 mV	1.2 V
sig_oa4p	17	HSCTRL8	50	Input	LVDS	250.0 mV	1.2 V
sig_oa3m	20	HSCTRL10	50	Input	LVDS	250.0 mV	1.2 V
sig_oa3p	21	HSCTRL11	50	Input	LVDS	250.0 mV	1.2 V
sig_oa2m	24	HSCTRL13	50	Input	LVDS	250.0 mV	1.2 V
sig_oa2p	25	HSCTRL14	50	Input	LVDS	250.0 mV	1.2 V
sig_oa1m	27	HSCTRL16	50	Input	LVDS	250.0 mV	1.2 V
sig_oa1p	29	CLK2_Out_p	50	Input	LVDS	250.0 mV	1.2 V
sig_ob4m	49	D07_Out_p	50	Input	LVDS	250.0 mV	1.2 V
sig_ob4p	50	D07_Out_n	50	Input	LVDS	250.0 mV	1.2 V
sig_ob3m	52	D08_Out_n	50	Input	LVDS	250.0 mV	1.2 V
sig_ob3p	54	D09_Out_p	50	Input	LVDS	250.0 mV	1.2 V
sig_ob2m	65	D11_Out_p	50	Input	LVDS	250.0 mV	1.2 V
sig_ob2p	66	D11_Out_n	50	Input	LVDS	250.0 mV	1.2 V
sig_ob1m	71	D13_Out_n	50	Input	LVDS	250.0 mV	1.2 V
sig_ob1p	73	D14_Out_p	50	Input	LVDS	250.0 mV	1.2 V
Outputs:							
Data outputs: (has on chip source termination)							
lvds_od1m	129	D09_In_n	50	Output	LVDS	250.0 mV	1.2 V
lvds_od1p	130	D09_In_p	50	Output	LVDS	250.0 mV	1.2 V
lvds_od2m	135	D07_In_p	50	Output	LVDS	250.0 mV	1.2 V
lvds_od2p	137	D06_In_n	50	Output	LVDS	250.0 mV	1.2 V
lvds_od3m	140	D05_In_p	50	Output	LVDS	250.0 mV	1.2 V
lvds_od3p	142	D04_In_n	50	Output	LVDS	250.0 mV	1.2 V
lvds_od4m	144	D03_In_n	50	Output	LVDS	250.0 mV	1.2 V
lvds_od4p	145	D03_In_p	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc1m	155	CLK2_In_p	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc1p	157	HSCTRL17	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc2m	159	HSCTRL19	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc2p	160	HSCTRL20	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc3m	163	HSCTRL22	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc3p	164	HSCTRL23	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc4m	167	HSCTRL25	50	Output	LVDS	250.0 mV	1.2 V
lvds_oc4p	168	HSCTRL26	50	Output	LVDS	250.0 mV	1.2 V

	Package pin	*Test board pin*	***Reff to VTT***	***Input / Output***	***Type***	***Swing***	***Common mode***
Control voltages:							
Clock input slew rate control:							
pscn_el	240	PDIN6-	NA	Input	Control	Analog	NA
pscn_op	241	PDIN6+	NA	Input	Control	Analog	NA
Clock duty cycle control:							
BIAS_CONTE	14	HSCTRL5	NA	Input	Control	Analog	NA
BIAS_CONTO	22	HSCTRL12	NA	Input	Control	Analog	NA
Clock delay chain control:							
VPP1	9	HSCTRL1	NA	Input	Control	Analog	1.2 V
VNN1	10	HSCTRL2	NA	Input	Control	Analog	1.2 V
VPP_EL	242	PDIN7-	NA	Input	Control	Analog	1.2 V
VNN_EL	243	PDIN7+	NA	Input	Control	Analog	1.2 V
Control inputs:							
Input interface clock select: (Used to by pass the delay chain)							
SEL_ELEC	12	HSCTRL4	NA	Input	Control	CMOS level	NA
SEL_OPT	19	HSCTRL9	NA	Input	Control	CMOS level	NA
Input interface phase select (used to change the input clock by 180 degrees)							
PHI1_A	26	HSCTRL15	NA	Input	Control	CMOS level	NA
PHI_A	30	CLK2_Out_n	NA	Input	Control	CMOS level	NA
Internal clock select (Used to selects the internal switch clock from optical or electrical clock)							
INT_SEL2	162	HSCTRL21	NA	Input	Control	CMOS level	NA
INT_SEL1	165	HSCTRL24	NA	Input	Control	CMOS level	NA
Switch control (Control inputs for the switch core setup)							
C0	47	D06_Out_n	NA	Input	Control	CMOS level	NA
C1	42	D04_Out_n	NA	Input	Control	CMOS level	NA
C2	44	D05_Out_p	NA	Input	Control	CMOS level	NA
C3	31	D00_Out_p	NA	Input	Control	CMOS level	NA
C4	11	HSCTRL3	NA	Input	Control	CMOS level	NA
C5	75	D15_Out_p	NA	Input	Control	CMOS level	NA
C6	173	HSCTRL30	NA	Input	Control	CMOS level	NA

BUSY BIT

Inputs:

			Reff to VTT	*Input / Output*	*Type*	*Swing*	*Common mode*
LVDS inputs:							
LVDS_BSp	76	D15_Out_n	50	Input	LVDS	500.0 mV	1.2 V
LVDS_BSm	78	C0_Out_p	50	Input	LVDS	500.0 mV	1.2 V
LVDS_Tp	86	C3_Out_n	50	Input	LVDS	500.0 mV	1.2 V
LVDS_Tm	88	FR_Out_p	50	Input	LVDS	500.0 mV	1.2 V
Control inputs:							
phase_sel	81	C1_Out_n	NA	Input	Control	CMOS level	NA
BIT1	94	CLK_In_p	NA	Input	Control	CMOS level	NA
BIT0	95	FR_In_n	NA	Input	Control	CMOS level	NA
MTm	116	D12_In_p	NA	Input	Control	CMOS level	NA
grab_reset2	170	HSCTRL28	NA	Input	Control	CMOS level	NA
grab_set2	172	HSCTRL29	NA	Input	Control	CMOS level	NA
TC2p	174	HSCTRL31	NA	Input	Control	CMOS level	NA
REQSET2	175	HSCTRL32	NA	Input	Control	CMOS level	NA
REQRESET2	187	PDOUT6+	NA	Input	Control	CMOS level	NA
clkock_in2	188	PDOUT6-	NA	Input	Control	CMOS level	NA

Outputs:

LVDS outputs: (LVDS outputs for BUSY BIT have on chip source termination)							
LVDSO_BSm	104	C1_In_p	50	Output	LVDS	500.0 mV	1.2 V
LVDSO_BSp	105	C0_In_n	50	Output	LVDS	500.0 mV	1.2 V
LVDSO_TOm	113	D13_In_n	50	Output	LVDS	500.0 mV	1.2 V
LVDSO_TOp	114	D13_In_p	50	Output	LVDS	500.0 mV	1.2 V
LVDS_TOm	118	D11_In_n	50	Output	LVDS	500.0 mV	1.2 V
LVDS_TOp	119	D11_In_p	50	Output	LVDS	500.0 mV	1.2 V
Grab outputs: (These outputs does not have on chip termination, depending on the requirement the rec							
grab_out0	96	FR_In_p	-	Output	-	2.0 V / 800 mV	1.2 V
grab_out1	98	C3_In_n	-	Output	-	2.0 V / 800 mV	1.2 V
grab_out2	99	C3_In_p	-	Output	-	2.0 V / 800 mV	1.2 V
grab_out3	100	C2_In_n	-	Output	-	2.0 V / 800 mV	1.2 V

2.0 V for no termination, 800 mV for 50 Ohm destination termination
Actual measurements suggest 240 mV for 50 Ohm termination

1.5 Testing of the Switch IC

Functional testing of the data path

The first test of the IC determined the sensitivity and phase margin of each individual channel of both the ports and paths at BER = 10^{-12} for 2^{31}-1 PRB NRZ, 2.0 Gb/s.

Summary of figures:

- Figure TE03_35.1 shows eye measurements at 2.25 Gb/s.
- Figure TE03_35. shows the output jitter 2.25 Gb/s.
- Figure TE03_35.3 shows the best- and worst- case input sensitivity at 2.0 Gb/s.
- Figure TE03_35.4 shows source-referred jitter of the electrical clock referenced to the input electrical clock at 1.3 GHz.

Table 3 summaries the TE03_35 measurement results.

Table 3: Summary of measurements

Measurement	Best		Worst	
	Value	Signal line	Value	Signal line
Input sensitivity	45 mVpp	lvds_ob1	65 mVpp	lvds_ob4
Power supply	3.3 V			
Power supply current	1.1 A			
VTT	1.2 V			
VTT current	0.3 A			
Data rate	2.25 Gb/s (data path), 2.0 Gb/s (BUSY BIT)			
Grab out	2.3 V(no termination), 240 mV (50 Ohm termination)			

1.0 2.25 Gb/s eye measurements

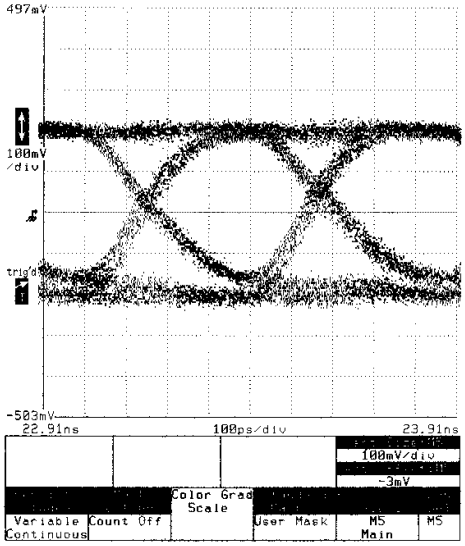
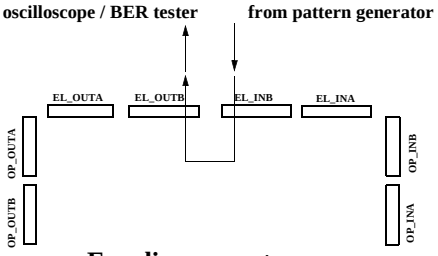


FIGURE TE03_35.1: Output eye diagram at 2.25 Gb/s (444 ps bit period, 250 mVpp input, 100 ps/div, 100 mV/div)

DATA RATE: 2.0 Gb/s

V_{DD} = 3.30 V
V_{TTin} = 1.20 V
V_{TTout} = 1.20 V
V_{in} = 250 mV_{pp}



Eye diagram setup

Input node = electrical B<4>
Output node = electrical B<4>

Data window = 444 ps
PRBS: 2^{31}-1 NRZ

EYE-WIDTH = 327 ps
EYE-HEIGHT = 185 mV
measured at BER = 10^{-3}

2.0 2.25 Gb/s jiter measurements

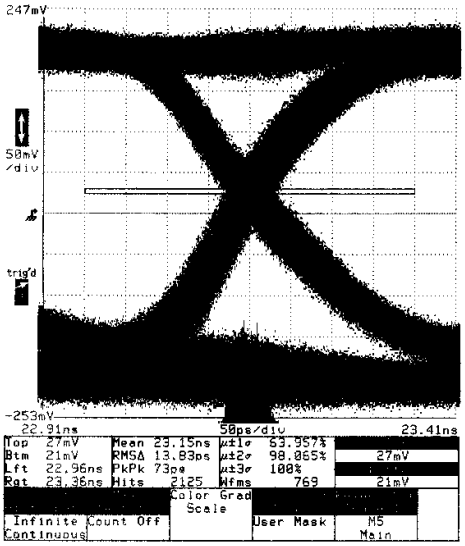


FIGURE TE03_35.2: Output jitter at 2.25 Gb/s (444 ps bit period, 250 mVpp input, 50 ps/div, 50 mV/div)

DATA RATE: 2.0 Gb/s

V_{DD} = 3.30 V
V_{TTin} = 1.20 V
V_{TTout} = 1.20 V
V_{in} = 250 mV_{pp}

Input node = electrical B<3>
Output node = electrical B<3>

Peak to Peak Jitter = 73.0 ps
RMS Jitter = 14.0 ps
PRBS: 2^{31}-1 NRZ

3.0 2.0 Gb/s input sensitivity

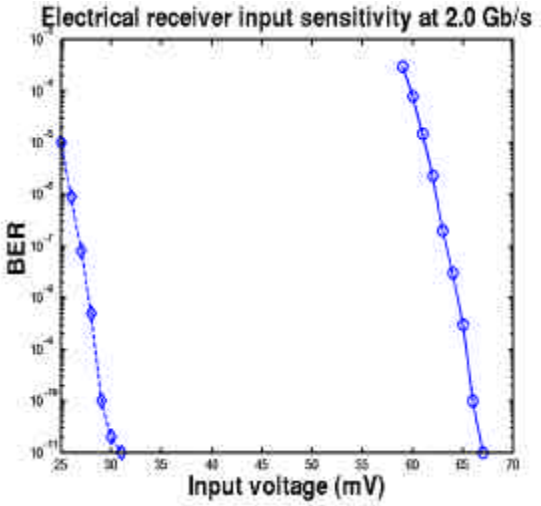


FIGURE TE03_35.3: Measured best and worst case input sensitivity of TE03_35 at 2.0 Gb/s (400 ps/ bit)

Better than 72 mVpp input sensitivity through insert and better than 67 mVpp input sensitivity direct wire bond, at BER = 10^{-11} NRZ 2^{31}-1 PRBS. Input common-mode voltage is 1.20 V.

The 88 Ω termination resistance generates 27% reflection at the input

4.0 1.3 GHz (2.6 Gb/s)source referred clock Jitter

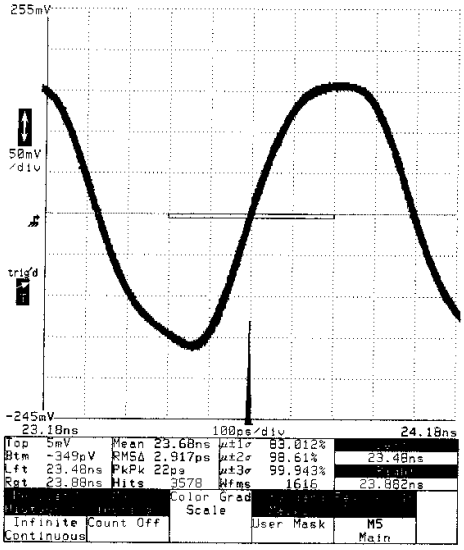


FIGURE TE03_35.4: Electrical output clock jitter referenced to the electrical input clock.

Clock frequency 1.3 GHz

V_{DD}	= 3.30 V
V_{TTin}	= 1.20 V

INT_SEL1	= 0.0 V
pscn_el	= 2.6 V
BIAS_CONTE	= 1.2 V
SEL_ELEC	= 0.0 V
PHI_A	= 0.0 V

Peak to peak jitter	= 22 ps
RMS jitter	= 3.0 ps

The self referred jitter of the pattern generator was measured at 20.0 ps peak to peak and 2.8 ps RMS.

When the switch was clocked using the input electrical clock (INT_SEL1 = INT_SEL2 = 0.0 V), the jitter of the electrical output clock and mock optical output clock referenced to the input clock were 3.0 ps and 2.8 ps RMS and 22 ps and 22 ps peak-to-peak. When the switch was clocked using the input optical (mock optical) clock (INT_SEL1 = INT_SEL2 = 3.3 V), the jitter of the electrical output clock and mock optical output clock referenced to the input clock were 1.5 ps and 2.6 ps RMS and 8 ps and 20 ps peak-to-peak.

BUSY BIT testing

The testing of the BUSY BIT circuitry is broken into four categories

- ***Frame logic test***
  The FRAME logic test includes testing the three different modes of FRAME operation.

  Pass-through mode (Figure TE03_35.5, Figure TE03_35.6 and Figure TE03_35.8 through Figure TE03_35.15): If the current node (switch) is not the master (MTm = 1), then regardless of the value of the FRAME creation input (TCp), the switch always remains in pass-through mode. If the current node is the master (MTm = 0), then if the FRAME creation input is not set (TCp = 0), then the switch remains in pass-through mode. In pass-through mode the output FRAME mirrors the input FRAME.

  Reset mode (Figure TE03_35.7): During reset mode, the output FRAME is zero regardless of the input FRAME. If the current node is the master (MTm = 0), and if the FRAME creation input is set (TCp = 1), then the switch is in reset mode.

  Creation mode: During creation mode, if the input FRAME is low, then it creates a new FRAME depending on the values in the BUSY BIT registers. If the current node is the master (MTm = 0), and if the input FRAME = 0, and if the FRAME creation input changes from one to zero (TCp 1 $\rightarrow$ 0), the switch enters into creation mode.
  Since creation mode requires that the input FRAME be zero ("0"), it is important that the master resets the FRAME for a long enough time so that the FRAME is reset throughout the network (ring). In order to create a FRAME, before the transition of the FRAME create input, one or more of the request interface registers should be set (starting with request interface register <3> (BS<3>).
  The length of the created FRAME is set to the number of request bits set starting from B<3> + 1. Thus, if only one request bit (B<3>) is set, then the length of the created FRAME is 2, corresponding to a 2-processor network.

- ***Encode, decode, and inversion control logic test***
  The successful decoding of complex encoded inputs are shown in Figure TE03_35.5 and Figure TE03_35.6. The successful operation of encoding for FRAME and BUSY are seen in the BUSY BIT request/grab and request/grab/release tests (Figure TE03_35.8 through Figure TE03_35.15).

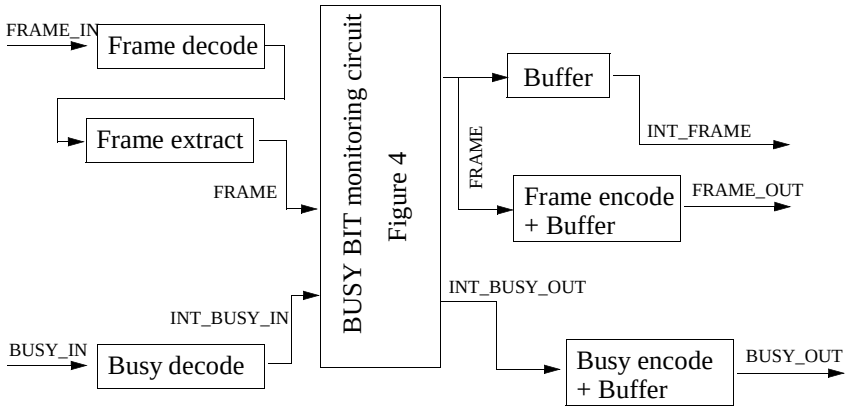
- **BUSY BIT logic test**
  BUSY BIT testing includes BUSY BIT pass-through, and BUSY BIT grab and release (Figure TE03_35.8 through Figure TE03_35.15.

- External interface (busy interface registers, grab interface registers and clocking them)

- During the test and measurements of the TE02 FRAME creation mode logic was tested. Since there were strength (pull-down) problems with the request and grab interface and grab interface registers a complete test of the BUSY BIT logic - including grab and release with grab interface register outputs could not be performed. During the BUSY BIT test of TE03_35 particular attention was given to verifying that the request and grab interface worked properly, and that the grab and release worked properly. The proceeding results will also concentrate on request and grab interface as well as the request, gran and release of BUSY BITs.

This set of measurements demonstrates correct decoding, inversion_control (phase_select) and FRAME pass-through mode operation.

- If the master is low (MTm = 1), or if master and FRAME control are both low (TCp,MTm = 0,1), the FRAME extraction circuitry will be in pass-through mode.
- If master and FRAME control are both high (Tcp,MTm = 1,0) and one or more Busy Requests including B<3> are set and TCp has a 1 → 0 transition, the circuit will be in pass-through mode after FRAME creation



5.0 Decoding, pass-through and invertion

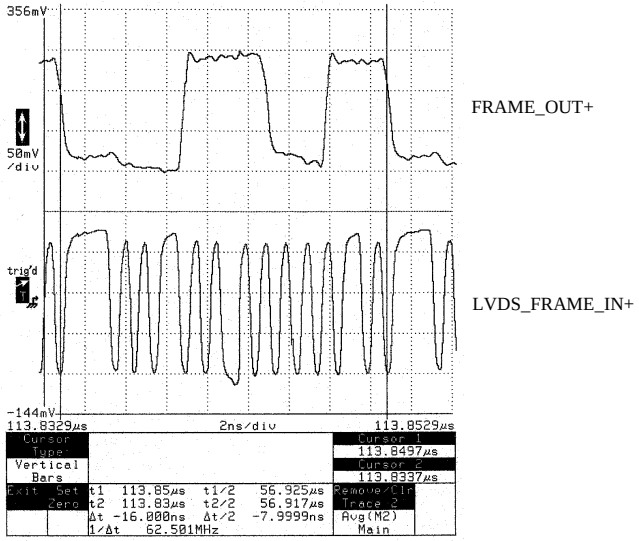


FIGURE TE03_35.5: Decode example #1.

Clock frequency 1.0 GHz (2.0 Gb/s)

- In this example the switch is set for FRAME pass-through. The following patterned is sent as the LVDS_FRAME +/-
  01111010101101010010101010101101 (32 bits)
- There are 2 possible decoding for the above input
  Possibility #1: 0001110000001111 (16 bits) &
  Possibility #2: 0011111000111111 (16 bits)
- The example shows the decoding for the possibility #2.
- phase_select (inversion control) = 0.0V

6.0 Encoding and pass-through of a 3-bit FRAME

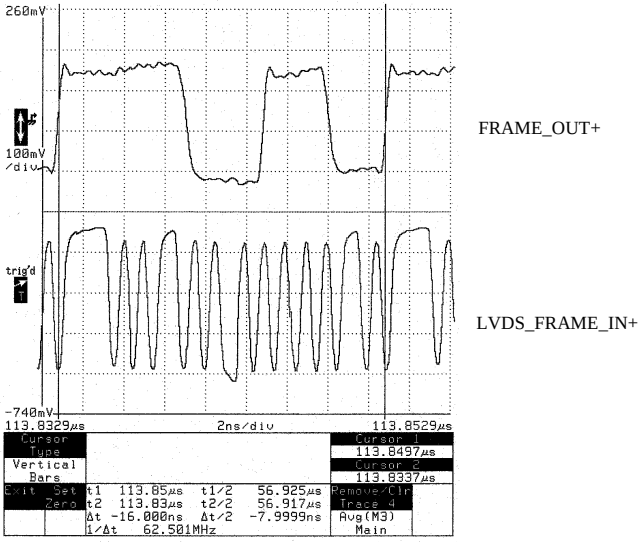


FIGURE TE03_35.6: Encode example #2

Clock frequency 1.0 GHz (2.0 Gb/s)

- The example shows the decoding for the possibility #2.
- phase_select (inversion control) = 3.3 V
- The decode FRAME is the inverted version of the example #1 (Figure TE03_35.5).

This set of measurements demonstrates the functionality FRAME reset logic.

- MTm = 0 identifies this as the master switch with the right to reset/create the FRAME.
- If the master and FRAME control are both high (TCp,MTm = 1,0), the internal FRAME will be zero regardless of the input FRAME.

7.0 Example of FRAME reset control

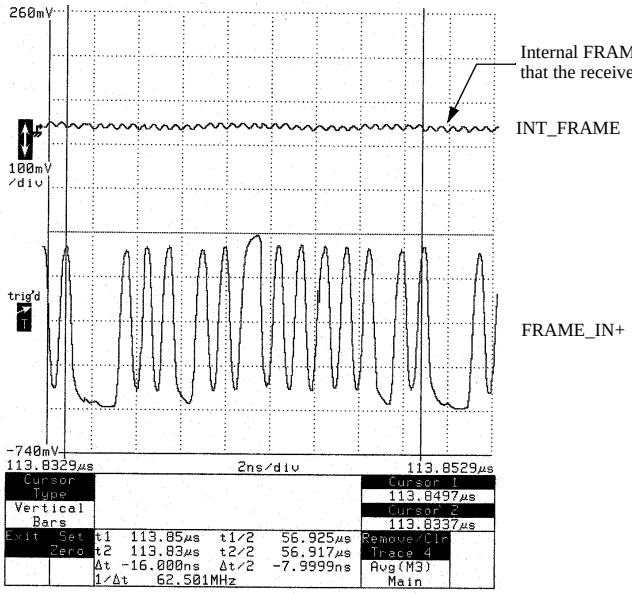


FIGURE TE03_35.7: Frame reset example.

Clock frequency 1.0 GHz (2.0 Gb/s)

- In this example continuously changing input is sent on FRAME_IN+/-.
- Since MS = 0 (active low), and TCp = 1 regardless of the input the internal FRAME is always zero.
- As a result the decoded FRAME output FRAME_OUT is zero.

This set of measurements demonstrates the functionality of the BUSY BIT request circuitry, request register and the request external interface.

- The switch is set for FRAME pass-through (MTm = 1,TCp = 0).
- An encoded output is generated by the pattern generator (DataOut +/-). The positive output (DataOut+) is used for FRAME_IN+ and the complement (DataOut-) is used for BUSY_IN+.
- When the FRAME_IN+ is decoded by the receive circuitry it creates a 4 bit wide FRAME, and since the complement is sent as the BUSY_IN the decoded busy input (received BUSY BIT input) will be the exact complement of the FRAME input.

8.0 Request register and BUSY grab test setup

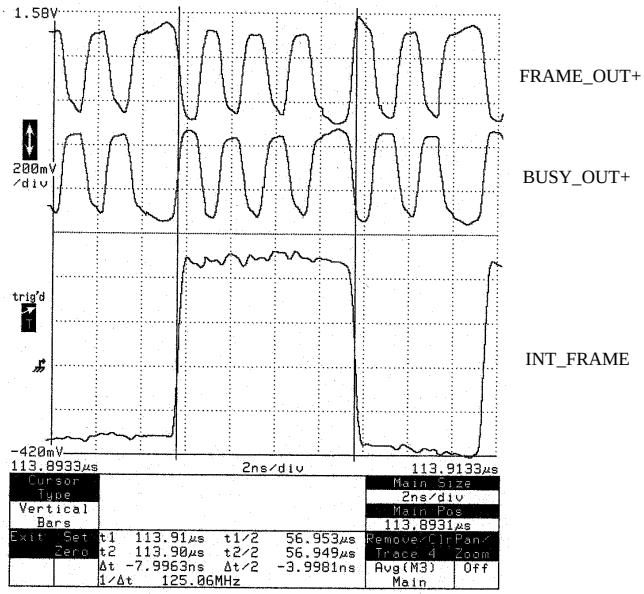


FIGURE TE03_35.8: The test setup for testing the request registers, request external interface and request and grab of BUSY BIT.

Clock frequency 1.0 GHz (2.0 Gb/s)

- Initially there are no requests. Thus the BUSY is also in pass-through (The output BUSY will mirror the BUSY input).
- The output shows that currently all the input BUSY BITs are free (BUSY_IN is zero during FRAME).

	Input	Output
FRAME	..01111 0..	..01111 0..
BUSY IN	..10000 1..	
BUSY OUT		..10000 1..

9.0 Requesting and grabbing #3

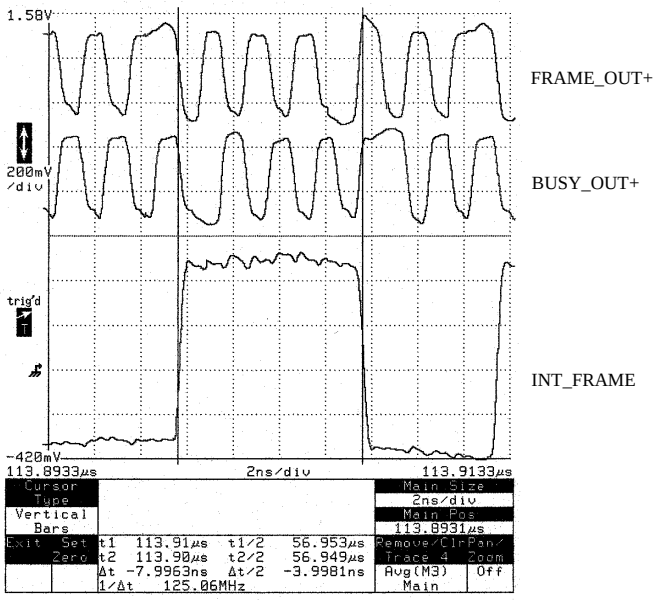


FIGURE TE03_35.9: Requesting and grabbing BUSY BIT <3>.

Clock frequency 1.0 GHz (2.0 Gb/s)

- The node is requestng BUSY BIT <3>, thus the BUSY output should change from 0000 to 1000
- The request for bit #3, is done by setting the external control signals BIT1 & BIT0 to 1 (3.3V) and then sending a short active high pulse on REQSET.

	Input	Output
FRAME	..01111 0..	..01111 0..
BUSY IN	..10000 1..	
BUSY OUT		..11000 1..

This is a continuation of the measurements demonstrates the functionality of the BUSY BIT circuit when no requests are being made.

- As seen in Figure TE03_35.10 when a request for bit #1 was made without resetting the request for bit #3, as expected, the circuitry was requesting and grabbing both bit #3 and bit #1.
- But when request for bit #1 was reset and request was made for #2, as expected, it stopped requesting bit #1, started requesting bit #2, and continued requesting bit #3.
- This test shows that the request registers and the request external interface works properly.

10.0 Requesting and grabbing #1 and #3

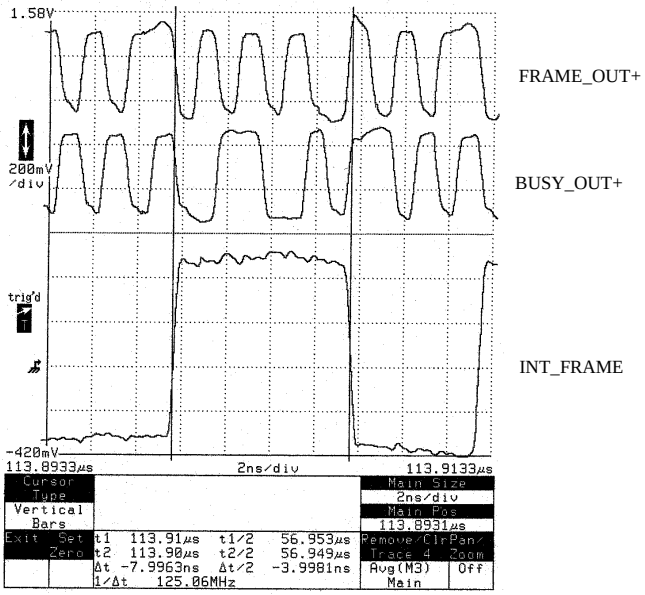


FIGURE TE03_35.10: The test setup for testing the request registers, request external interface and request and grab of BUSY BIT.

Clock frequency 1.0 GHz (2.0 Gb/s)

- Request bit #1, without resetting the request for bit #3.
- Since the node is requesting BUSY BIT <3> and BUSY BIT <1> the output should change to 1010.

	Input	Output
FRAME	..011110..	..011110..
BUSY IN	..100001..	
BUSY OUT		..110101..

11.0 Requesting and grabbing #1 and #2

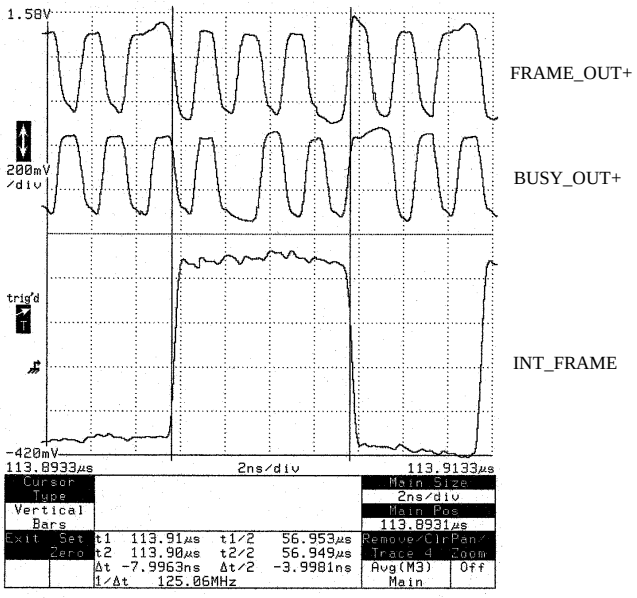


FIGURE TE03_35.11: Requesting and grabbing BUSY BIT <3>.

Clock frequency 1.0 GHz (2.0 Gb/s)

- Reset the request for bit #1, and request #2.
- Since the node is requesting BUSY BIT <3> and BUSY BIT <1> the output should change to 1100.

	Input	Output
FRAME	..011110..	..011110..
BUSY IN	..100001..	
BUSY OUT		..111001..

This a set of measurements to show the test for proper operation of request, grab and release, as well as the grab register external interface. Showing request, grab and release is sufficient to conclude that the grab registers are working properly.

- An encoded input that decodes to 2 consecutive 4 bit wide FRAMEs are sent on FRAME_IN.
- During the first FRAME all zeros (all BUSY BITs free) are sent on BUSY IN.
- During the second FRAME all but BUSY IN <3> is zero (BUSY BIT<3> not free, BUSY BIT <2:0> are free).

12.0 Set up for request, grab and release test

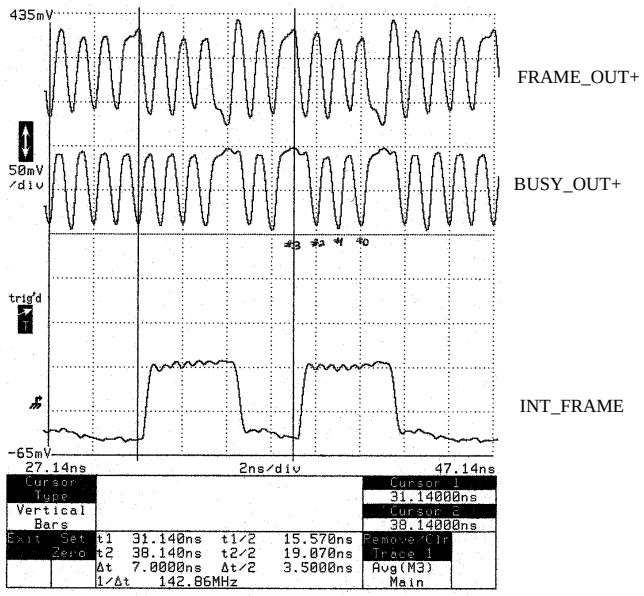


FIGURE TE03_35.12: The test setup for testing the request/grab and release of BUSY BIT.

13.0 Comparison test: Bit #1 continuously requested.

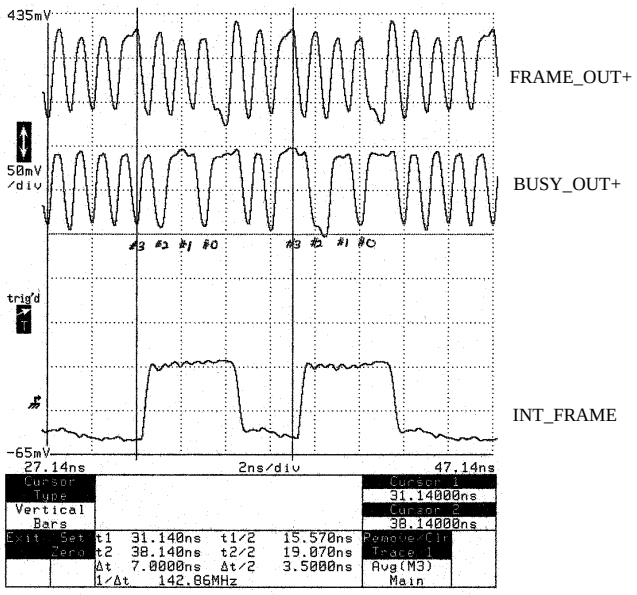


FIGURE TE03_35.13: Requesting and grabbing BUSY BIT <3>.

Clock frequency 1.0 GHz (2.0 Gb/s)

- The node (switch) is not requesting any bits.
- Output BUSY should mirror the input.

	Input	Output
FRAME	..011110..	..011110..
#1 FRAME BUSY IN	..100001..	
BUSY OUT		..100001..
#1 FRAME BUSY IN	..110001..	
BUSY OUT		..110001..

Clock frequency 1.0 GHz (2.0 Gb/s)

- Continuously requesting bit #1
- Since the node is requesting BUSY BIT <1> during the 1st FRAME the output BUSY should be 0010, and during the 2nd FRAME the output should be 1010.the output should change to 1100.
- This test does not have any "release" included, but was done before the bit #3 request/grab release to show that bit #1 request is different from bit #3 request.

	Input	Output
FRAME	..011110..	..011110..
#1 FRAME BUSY IN	..100001..	
BUSY OUT		..100101..
#1 FRAME BUSY IN	..110001..	
BUSY OUT		..110101..

This a continuation of the measurements to show the test for proper operation of request, grab and release, as well as the grab register external interface. Showing request, grab and release is sufficient to conclude that the grab registers are working properly.

- Since reqset get precedence over reqreset, reqreset is continuously kept high.
- When reset is set to high, the request bit indicated by bits BIT1 and BIT0 will be set, and when reqset is changed to zero, since reqreset is continuously high, the request bit will be reset.
- The above strategy was used to set and reset the request bit #3 in the following tests.

14.0 Request/grab and release of bit #3

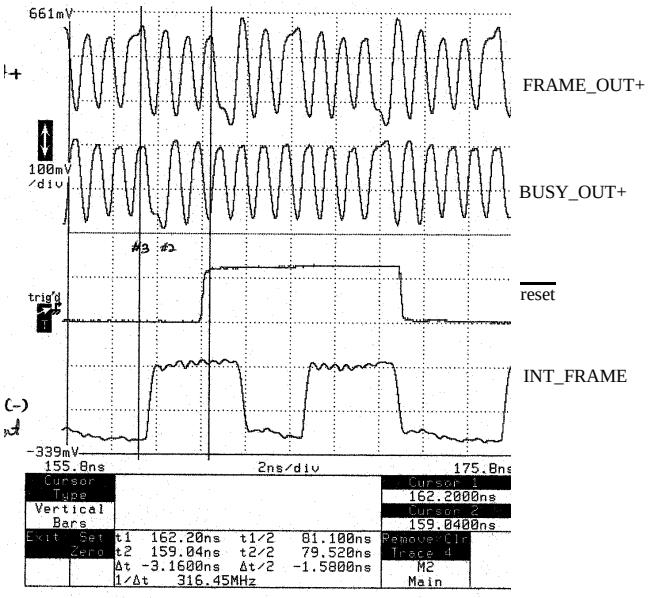


FIGURE TE03_35.14: Request/grab and release of bit #3 test outputs with reqset.

15.0 Grab register external interface test

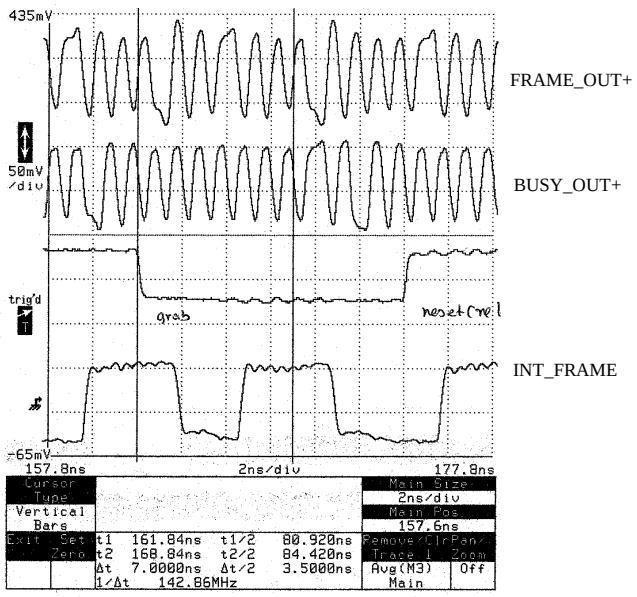


FIGURE TE03_35.15: Request, grab, release and grab register external interface test.

Clock frequency 1.0 GHz (2.0 Gb/s)

- During FRAME #1 requesting bit #3, and releases the request before FRAME #2.
- Since the node is requesting BUSY BIT <3> during the 1st FRAME the output BUSY should be 1000.
- Since the request for #3 is reset before 2nd FRAME, bit #3 should be released, so the BUS Y output should be 0000 (the input was 1000).

	Input	Output
FRAME	..011110..	..011110..
#1 FRAME BUSY IN	..100001..	
BUSY OUT		..11001..
#1 FRAME BUSY IN	..110001..	
BUSY OUT		..100001..

Clock frequency 1.0 GHz (2.0 Gb/s)

- The setup is quite similar to Figure TE03_35.14.
- Here the grab register output grab_out3 is shown.
- As expected after the 1st FRAME grab_out3 changes to low. Indicates that bit #3 was grabbed.
- After the 2nd FRAME grab_out3 changes to high. Indicates that bit #3 was released.

1.6 Discussion on testing:

1.6.1 Clock up test:

The first test that was performed is the clock up and operation test. This test verified proper operation of the different settings of the switch IC clocking and the clock tree design. It is important to ensure that the clock can be received and controlled properly prior to any other tests.

Table 4: Clock up test initial settings

Signal name	Voltage
VPP_EL	2.4 V
VNN_EL	0.0 V
VPP1	2.4 V
VNN1	0.0 V
pscn_el	2.6 V
pscn_opt	2.6 V
INT_SEL1	0.0 V
INT_SEL2	0.0 V
PHI_A	0.0 V
PHI1_A	0.0 V
BIAS_CONTE	1.0 V
BIAS_CONTO	1.2 V
VTT	1.2 V
SEL_ELEC	0.0 V
SEL_OPT	0.0 V

The above setting (INT_SEL1 and INT_SERL2) the internal switch clock is selected to be the received electrical clock. To test that the optical clock can be selected as the switch internal clock change values of INT_SEL1 and INT_SEL2. INT_SEL1 controls the clock chain #1 (Figure 2) and INT_SEL2 controls the clock chain #2.

1.6.2 Data path tests

The clock up test settings need not be changed unless one needs to experiment with the phase relationship control or delay chain by pass control. The control lines PHI_A and PHI1_A can be used to control the phase relationship between two input interfaces and the 2 internal clock trees (chain #1 and chain #2, Figure 2). The delay chain bypass controls are SEL_ELEC and SEL_OPT. When the delay chain is bypassed it is recommended that one retain the bias voltage of VPP_EL and VPP1 at the levels given in Table 4.

The control signals C0 - C6 controls the switch core and important control combinations are shown in Figure 3 and the relationship between the control lines and the switch core blocks are shown in Figure 2. An executable "CROSS-CONNECT" is available to the user to understand and experiment with the switch core setup.

1.6.3 BUSY BIT test

Please refer to the earlier section on BUSY BIT testing and BUSY BIT information. The grab_reset2 and grab_set2 signals will only be used if the user requires to reset or set all the grab registers. Even though it is recommended that one not activate a set and a reset at the same time, a "1" (3.3 V) on grab_set2 over rides a "1" on grab_reset2, and a "1" (3.3 V) on reqset2 will override a "1" on reqreset.

As indicated earlier the internal decoded FRAME monitoring output (LVDS_TOp and LVDS_TOm) polarity is reversed. There is also a maximum 3 cycle latency between the internal FRAME and the FRAME monitoring output.

1.7 General Discussion

The test results of TE03_35 shows 75 ps peak-to-peak output jitter for 2.25 Gb/s, 2^{31}-1 PRBS NRZ signaling rate and BER < 10^{-13}.

As in TE02, TE03_35 also has long on-chip wires. At present most literature assumes the RC delays of moderate length (few millimeters) on chip wires are much significantly greater than the flight times and models them as distributed RC lines. The above assumption is valid for lower level metal wiring. For wiring on higher layers of metals the area capacitance can be < 10% of the total capacitance, and depending on the wire spacing (wiring grid) and the wire width, moderate length onchip wires can have flight times that are comparable to their RC delays. Even in a Switch IC integrating CMOS with optics and such wire lengths can be expected, and thus needs to be modeled more accurately.

The BUSY BIT problems that were encountered in TE02 testing were no longer present in the TE03_35 testing. The measurements suggests that resizing of the RS latches in TE03_35 have fixed the TE02 NMOS pull-down problem. The output swing of the grab interface register output drivers did not match the process corner simulation results when they were terminated with 50 Ω termination resistors.

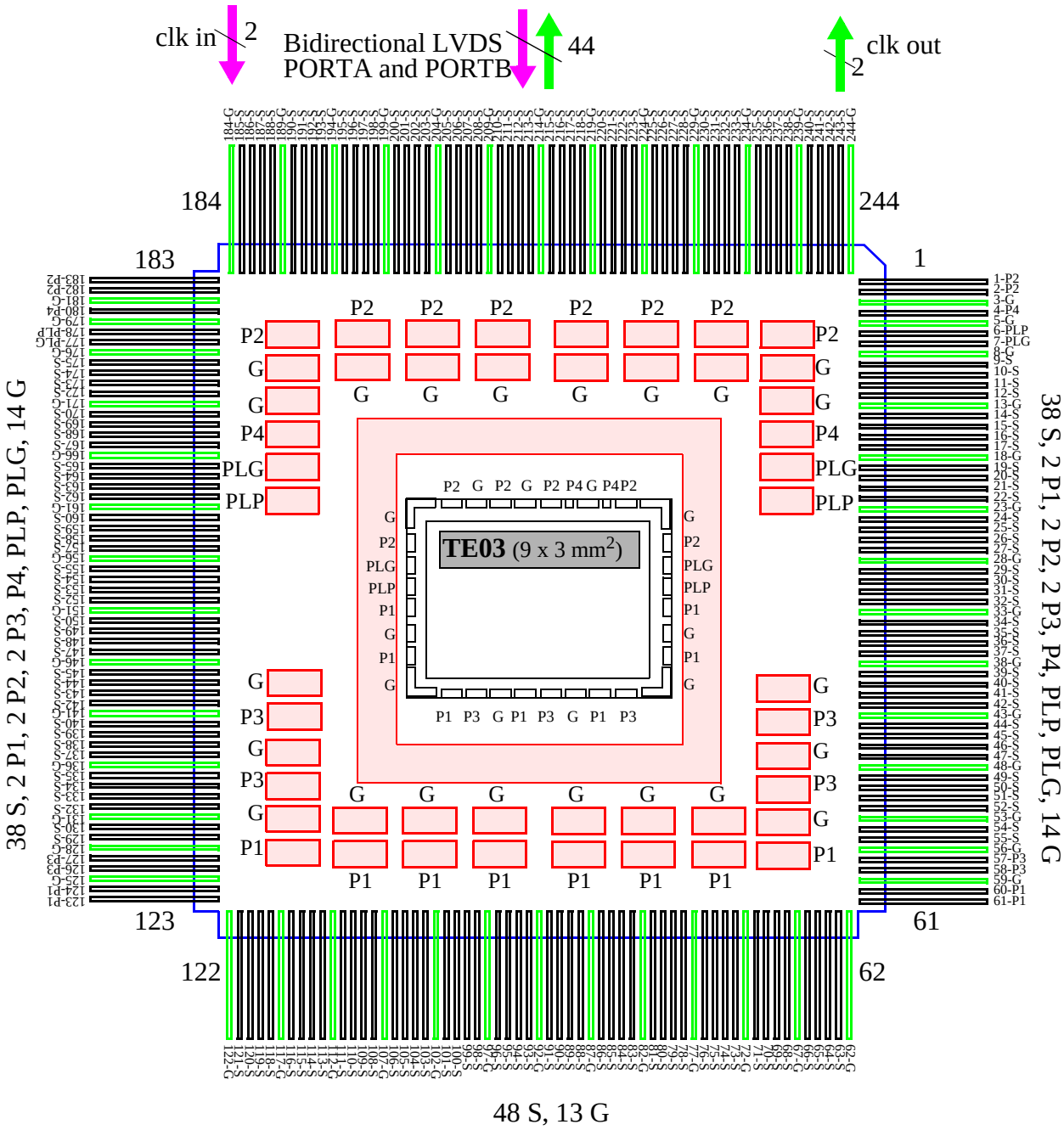
2.0 Glossary of Terms

- BOIC — Buffered optical input clock
- CMOS — Complementary metal oxide semiconductor
- Crossbar Circuit: — Includes the crossbar switch, mux/demux, clock tree, and control logic
- Crossbar Switch — Includes the switch core, the dynamic drivers, and the SAFFs. When one includes all three blocks, the logic scheme of the switch is defined as low swing differential pass transistor logic.
- CSL — Current steering logic
- CSL-SA — Current steering logic sense amp
- CSL-SR — Current steering logic set reset flip-flop
- CSL-SAFF — Current steering logic sense-amp flip-flop
- CSWL — Current switch logic
- DEMUX — De-multiplexer
- EIC — Electrical input clock
- FF — Flip-Flop
- GCSS — Global clocked synchronous switching
- HCI — Host control interface
- I/O — Input/Output
- LCAS — Local clocked asynchronous signaling
- LVDS — Low voltage differential swing
- Reference Switch IC — The Switch IC connected to the reference processor board
- MIN — Multistage interconnect network
- MUX — Multiplexer
- Network Reference: — Reference controller or processor for the total network
- NG Formatter — Northrop Grumman Formatter chip
- NOR — Negation of OR
- OIC — Optical input clock
- OOC — Optical output clock
- Path — At the optoelectronic interfaces, and within the Switch IC, a group of data signal lines assigned to a processor is called a path
- Port — At the electrical I/O interface a group of data signal lines assigned to a processor is called a port.
- SA — Sense-amp
- SAFF — Sense-amp flip-flop
- SRFF — Set reset flip-flop
- Switch core: — The five deep pass transistor block
- TSPC — True single phase clocking
- UAS — Unclocked asynchronous switching

3.0 Package diagrams

Further details of QFP:

Cavity up view lead assignments



CAVITY UP VIEW